FIG. 1

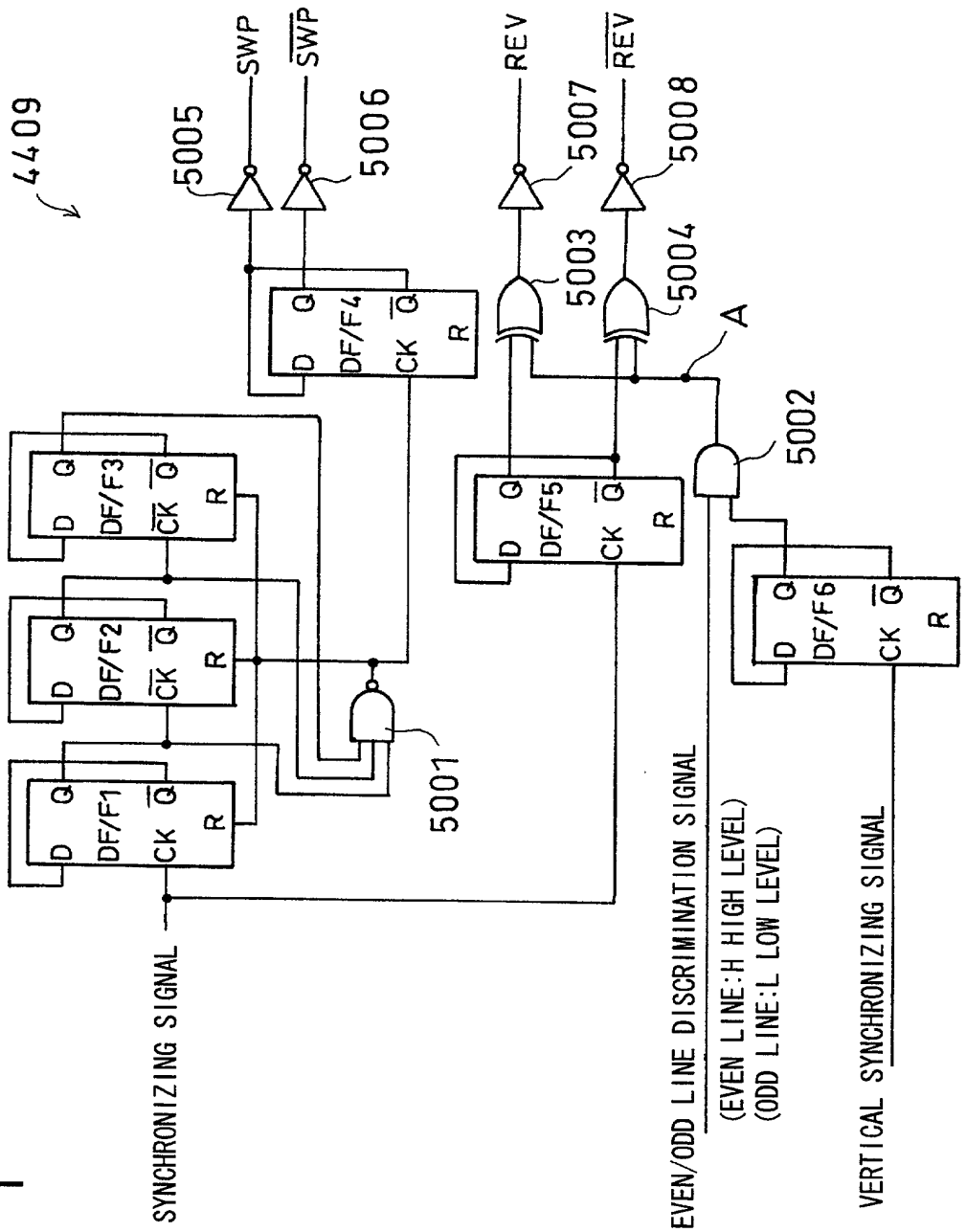

4409
5005
SWP
5006
SWP
5007
REV
5008
REV
5003
5004
A
5002
5001
DF/F1
DF/F2
DF/F3
DF/F4
DF/F5
DF/F6
D
Q
CK
R
HORIZONTAL SYNCHRONIZING SIGNAL
EVEN/ODD LINE DISCRIMINATION SIGNAL
(EVEN LINE:H HIGH LEVEL)
(ODD LINE:L LOW LEVEL)
VERTICAL SYNCHRONIZING SIGNAL

FIG. 2

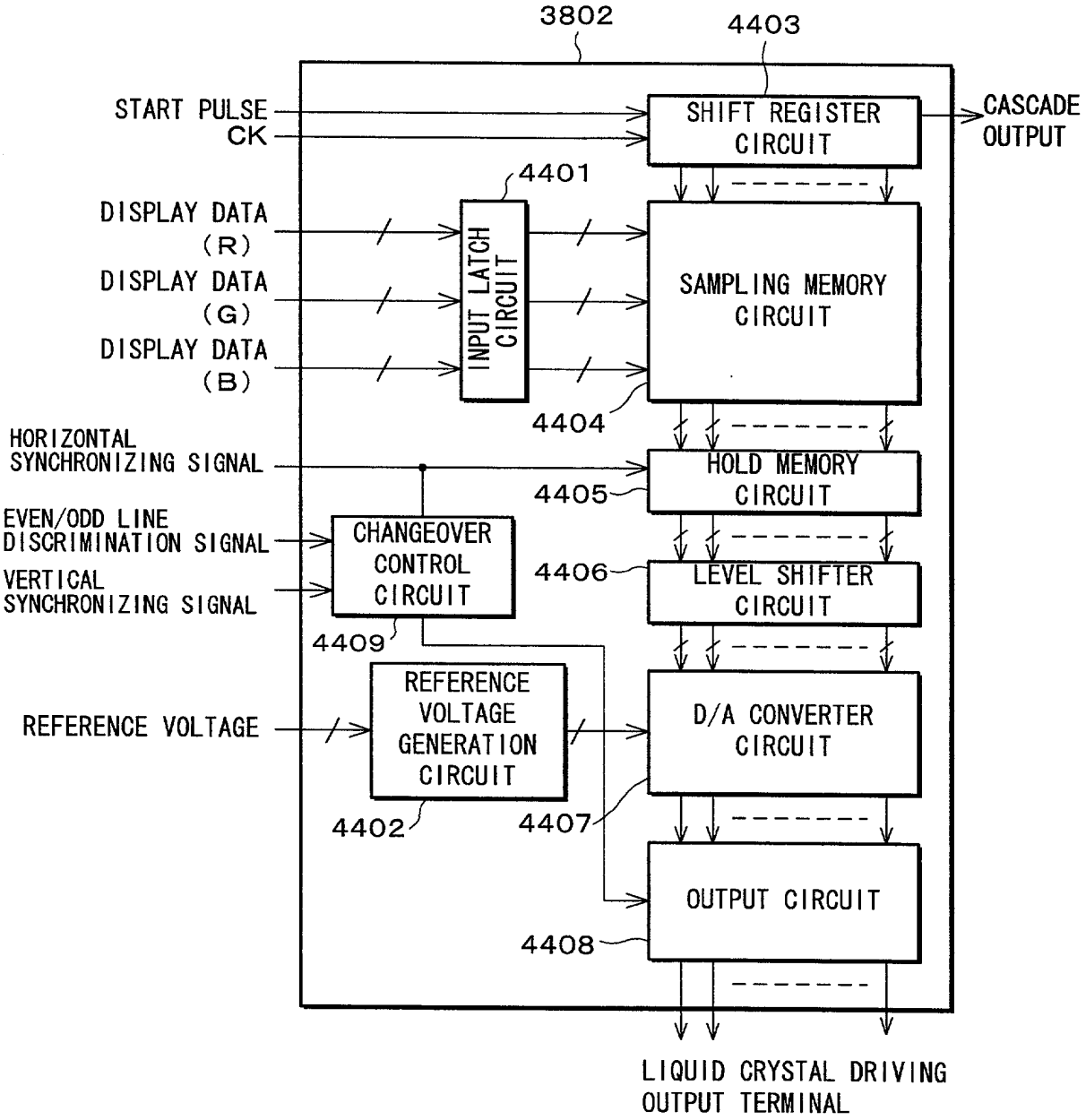

3802
4403
START PULSE
CK
SHIFT REGISTER CIRCUIT
CASCADE OUTPUT
4401
DISPLAY DATA (R)
DISPLAY DATA (G)
DISPLAY DATA (B)
INPUT LATCH CIRCUIT
SAMPLING MEMORY CIRCUIT
4404
HORIZONTAL SYNCHRONIZING SIGNAL
HOLD MEMORY CIRCUIT
4405
EVEN/ODD LINE DISCRIMINATION SIGNAL
VERTICAL SYNCHRONIZING SIGNAL
CHANGEOVER CONTROL CIRCUIT
4406
LEVEL SHIFTER CIRCUIT
4409
REFERENCE VOLTAGE
REFERENCE VOLTAGE GENERATION CIRCUIT
D/A CONVERTER CIRCUIT
4402
4407
OUTPUT CIRCUIT
4408
LIQUID CRYSTAL DRIVING OUTPUT TERMINAL

FIG. 3

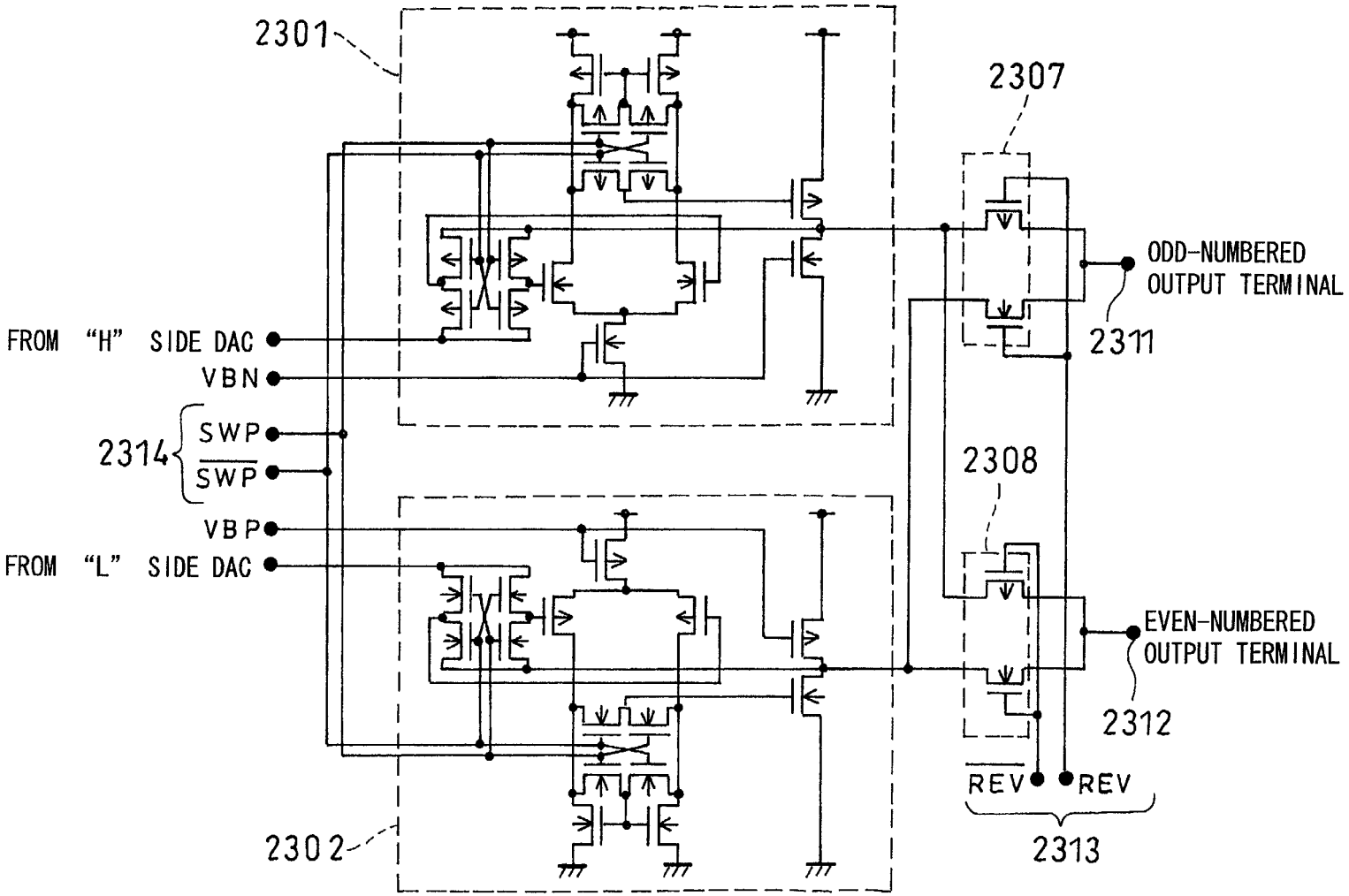

2301
2307
ODD-NUMBERED
OUTPUT TERMINAL
2311
FROM "H" SIDE DAC
VBN
2314
SWP
SWP
2308
VBP
FROM "L" SIDE DAC
EVEN-NUMBERED
OUTPUT TERMINAL
2312
REV
REV
2313
2302

FIG. 4

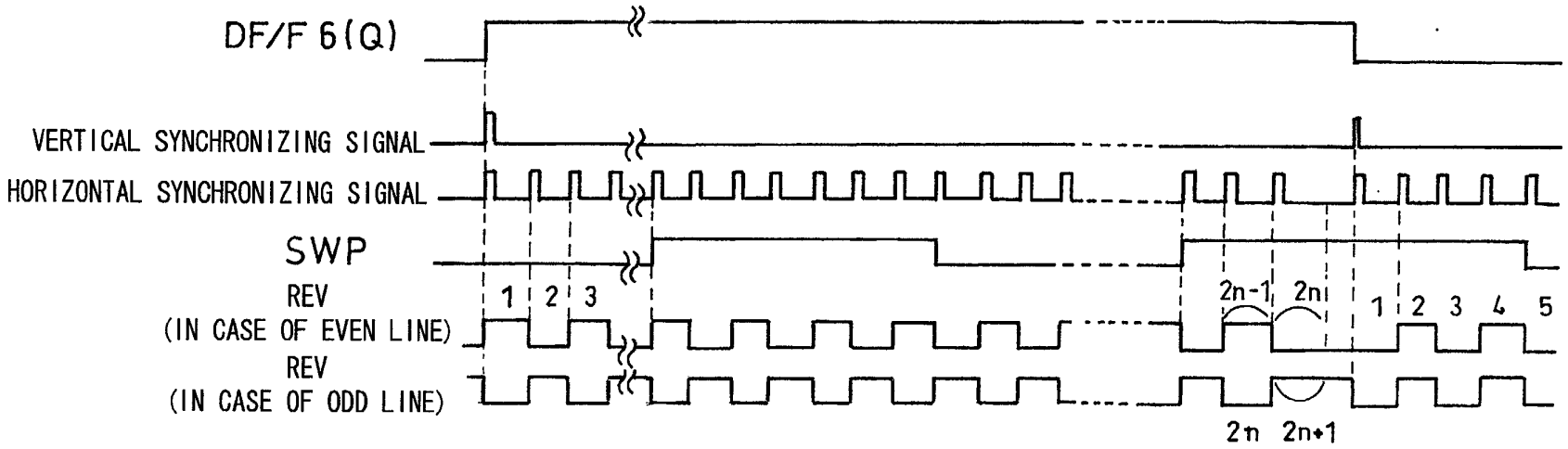

DF/F 6(Q)
VERTICAL SYNCHRONIZING SIGNAL
HORIZONTAL SYNCHRONIZING SIGNAL
SWP
REV
(IN CASE OF EVEN LINE)
REV
(IN CASE OF ODD LINE)
1
2
3
2n-1
2n
1
2
3
4
5
2n
2n+1

FIG. 5

① FRAME

EVEN LINE

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	+A	+B	+A	+B	+A	+B	+A	+B	L	L
②	+B	+A	+B	+A	+B	+A	+B	+A	H	L
③	+A	+B	+A	+B	+A	+B	+A	+B	L	L
④	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑤	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑥	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑦	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑧	-B	-A	-B	-A	-B	-A	-B	-A	H	H

② FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	-B	-A	-B	-A	-B	-A	-B	-A	H	H
②	-A	-B	-A	-B	-A	-B	-A	-B	L	H
③	-B	-A	-B	-A	-B	-A	-B	-A	H	H
④	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑤	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑥	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑦	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑧	+A	+B	+A	+B	+A	+B	+A	+B	L	L

③ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	+A	+B	+A	+B	+A	+B	+A	+B	L	L
②	+B	+A	+B	+A	+B	+A	+B	+A	H	L
③	+A	+B	+A	+B	+A	+B	+A	+B	L	L
④	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑤	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑥	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑦	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑧	-B	-A	-B	-A	-B	-A	-B	-A	H	H

④ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	-B	-A	-B	-A	-B	-A	-B	-A	H	H
②	-A	-B	-A	-B	-A	-B	-A	-B	L	H
③	-B	-A	-B	-A	-B	-A	-B	-A	H	H
④	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑤	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑥	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑦	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑧	+A	+B	+A	+B	+A	+B	+A	+B	L	L

⑤ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	+A	+B	+A	+B	+A	+B	+A	+B	L	L
②	+B	+A	+B	+A	+B	+A	+B	+A	H	L
③	+A	+B	+A	+B	+A	+B	+A	+B	L	L
④	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑤	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑥	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑦	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑧	-B	-A	-B	-A	-B	-A	-B	-A	H	H

⑥ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	-B	-A	-B	-A	-B	-A	-B	-A	H	H
②	-A	-B	-A	-B	-A	-B	-A	-B	L	H
③	+B	+A	+B	+A	+B	+A	+B	+A	H	L
④	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑤	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑥	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑦	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑧	+A	+B	+A	+B	+A	+B	+A	+B	L	L

⑦ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	+A	+B	+A	+B	+A	+B	+A	+B	L	L
②	-B	-A	-B	-A	-B	-A	-B	-A	H	H
③	-A	-B	-A	-B	-A	-B	-A	-B	L	H
④	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑤	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑥	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑦	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑧	-B	-A	-B	-A	-B	-A	-B	-A	H	H

A:VOLTAGE HAVING POSITIVE POLARITY
B:VOLTAGE HAVING NEGATIVE POLARITY

+:POSITIBE OFFSET
-:NEGATIVE OFFSET

⑧ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	+B	+A	+B	+A	+B	+A	+B	+A	H	L
②	+A	+B	+A	+B	+A	+B	+A	+B	L	L
③	+B	+A	+B	+A	+B	+A	+B	+A	H	L
④	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑤	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑥	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑦	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑧	-A	-B	-A	-B	-A	-B	-A	-B	L	H

⑨ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	-A	-B	-A	-B	-A	-B	-A	-B	L	H
②	-B	-A	-B	-A	-B	-A	-B	-A	H	H
③	-A	-B	-A	-B	-A	-B	-A	-B	L	H
④	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑤	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑥	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑦	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑧	+B	+A	+B	+A	+B	+A	+B	+A	H	L

⑩ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	+B	+A	+B	+A	+B	+A	+B	+A	H	L
②	+A	+B	+A	+B	+A	+B	+A	+B	L	L
③	+B	+A	+B	+A	+B	+A	+B	+A	H	L
④	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑤	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑥	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑦	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑧	-A	-B	-A	-B	-A	-B	-A	-B	L	H

⑪ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	-A	-B	-A	-B	-A	-B	-A	-B	L	H
②	-B	-A	-B	-A	-B	-A	-B	-A	H	H
③	-A	-B	-A	-B	-A	-B	-A	-B	L	H
④	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑤	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑥	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑦	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑧	+B	+A	+B	+A	+B	+A	+B	+A	H	L

⑫ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	+B	+A	+B	+A	+B	+A	+B	+A	H	L
②	+A	+B	+A	+B	+A	+B	+A	+B	L	L
③	+B	+A	+B	+A	+B	+A	+B	+A	H	L
④	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑤	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑥	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑦	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑧	-A	-B	-A	-B	-A	-B	-A	-B	L	H

⑬ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	-A	-B	-A	-B	-A	-B	-A	-B	L	H
②	-B	-A	-B	-A	-B	-A	-B	-A	H	H
③	+A	+B	+A	+B	+A	+B	+A	+B	L	L
④	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑤	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑥	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑦	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑧	+B	+A	+B	+A	+B	+A	+B	+A	H	L

⑭ FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	+B	+A	+B	+A	+B	+A	+B	+A	H	L
②	-A	-B	-A	-B	-A	-B	-A	-B	L	H
③	-B	-A	-B	-A	-B	-A	-B	-A	H	H
④	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑤	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑥	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑦	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑧	-A	-B	-A	-B	-A	-B	-A	-B	L	H

FIG. 6

VOLTAGE APPLIED TO PIXEL①－①

FRAME	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	⑫	⑬	⑭
	+A	−B	+A	−B	+A	−B	+A	+B	−A	+B	−A	+B	−A	+B

7 FRAME　　7 FRAME

FIG. 7

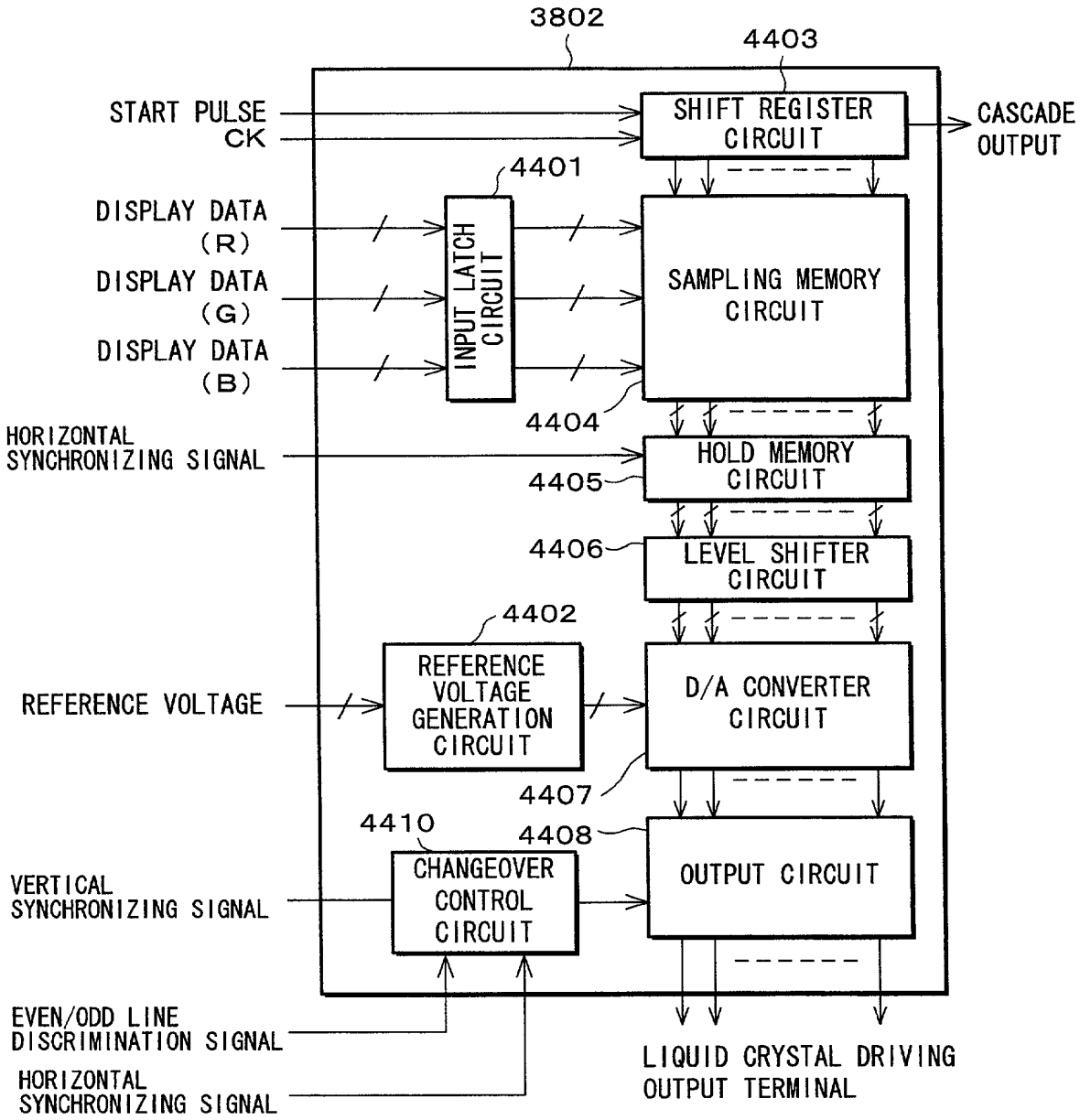

3802
4403
START PULSE
CK
SHIFT REGISTER CIRCUIT
CASCADE OUTPUT
4401
DISPLAY DATA (R)
DISPLAY DATA (G)
DISPLAY DATA (B)
INPUT LATCH CIRCUIT
SAMPLING MEMORY CIRCUIT
4404
HORIZONTAL SYNCHRONIZING SIGNAL
HOLD MEMORY CIRCUIT
4405
4406
LEVEL SHIFTER CIRCUIT
4402
REFERENCE VOLTAGE
REFERENCE VOLTAGE GENERATION CIRCUIT
D/A CONVERTER CIRCUIT
4407
4410
4408
VERTICAL SYNCHRONIZING SIGNAL
CHANGEOVER CONTROL CIRCUIT
OUTPUT CIRCUIT
EVEN/ODD LINE DISCRIMINATION SIGNAL
HORIZONTAL SYNCHRONIZING SIGNAL
LIQUID CRYSTAL DRIVING OUTPUT TERMINAL

FIG. 8

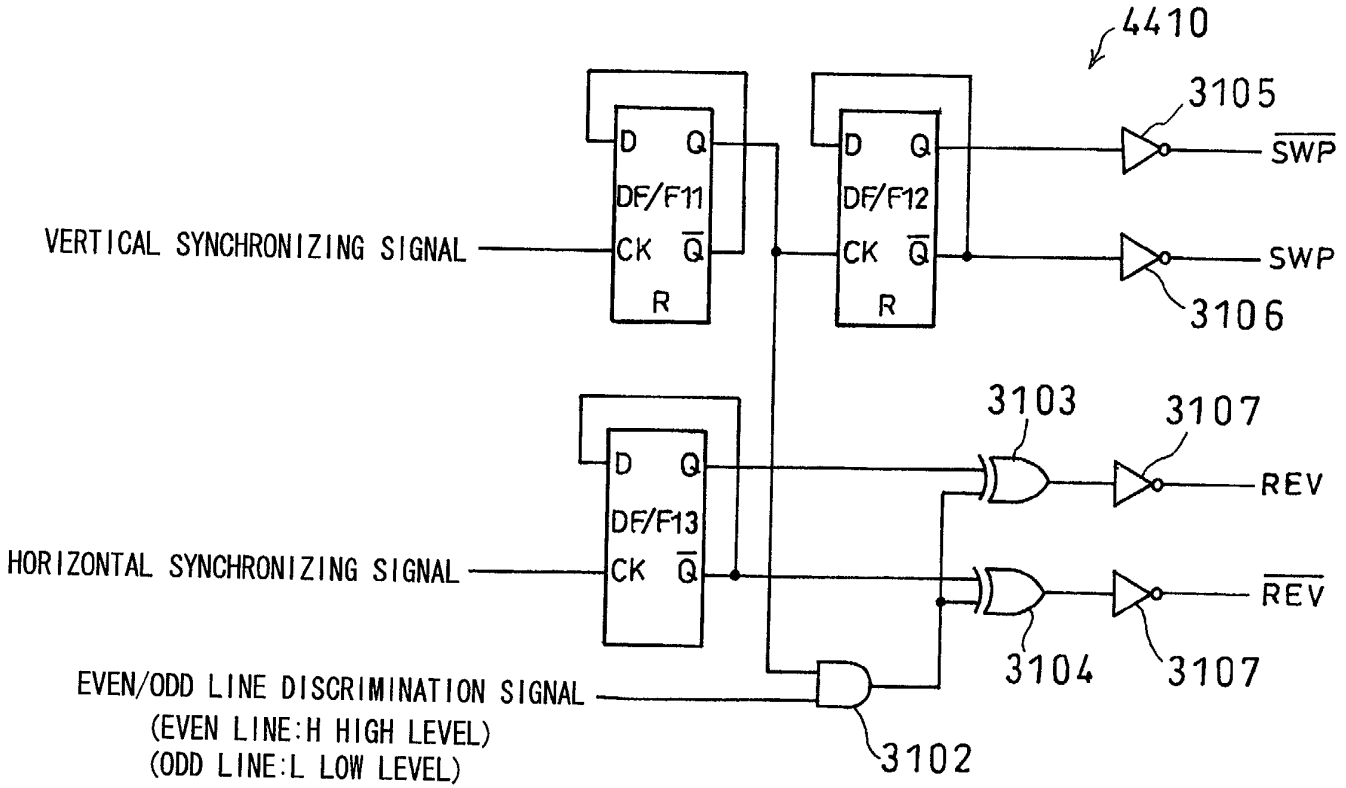

4410
3105
D Q
DF/F11
CK Q
R
D Q
DF/F12
CK Q
R
SWP
SWP
3106
VERTICAL SYNCHRONIZING SIGNAL
3103
3107
D Q
DF/F13
CK Q
REV
REV
HORIZONTAL SYNCHRONIZING SIGNAL
3104
3107
EVEN/ODD LINE DISCRIMINATION SIGNAL
(EVEN LINE:H HIGH LEVEL)
(ODD LINE:L LOW LEVEL)
3102

FIG. 9

1 FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	+A	+B	+A	+B	+A	+B	+A	+B	L	L
②	+B	+A	+B	+A	+B	+A	+B	+A	H	L
③	+A	+B	+A	+B	+A	+B	+A	+B	L	L
④	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑤	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑥	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑦	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑧	+B	+A	+B	+A	+B	+A	+B	+A	H	L

2 FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	+B	+A	+B	+A	+B	+A	+B	+A	H	L
②	+A	+B	+A	+B	+A	+B	+A	+B	L	L
③	+B	+A	+B	+A	+B	+A	+B	+A	H	L
④	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑤	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑥	+A	+B	+A	+B	+A	+B	+A	+B	L	L
⑦	+B	+A	+B	+A	+B	+A	+B	+A	H	L
⑧	+A	+B	+A	+B	+A	+B	+A	+B	L	L

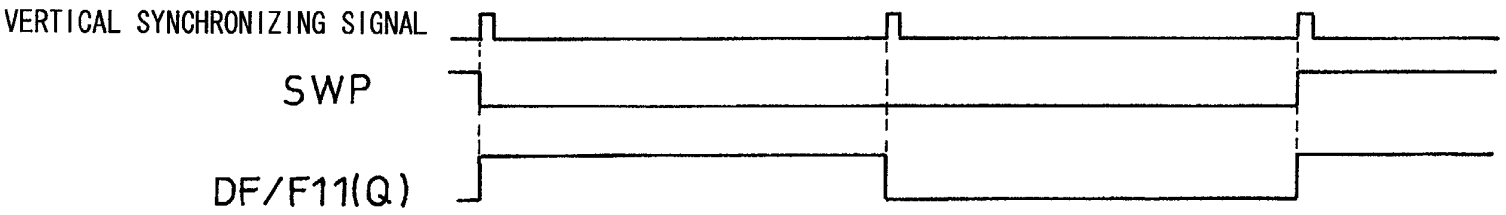
3 FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	-A	-B	-A	-B	-A	-B	-A	-B	L	H
②	-B	-A	-B	-A	-B	-A	-B	-A	H	H
③	-A	-B	-A	-B	-A	-B	-A	-B	L	H
④	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑤	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑥	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑦	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑧	-B	-A	-B	-A	-B	-A	-B	-A	H	H

4 FRAME

	①	②	③	④	⑤	⑥	⑦	⑧	REV	SWP
①	-B	-A	-B	-A	-B	-A	-B	-A	H	H
②	-A	-B	-A	-B	-A	-B	-A	-B	L	H
③	-B	-A	-B	-A	-B	-A	-B	-A	H	H
④	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑤	-B	-A	-B	-A	-B	-A	-B	-A	H	H
⑥	-A	-B	-A	-B	-A	-B	-A	-B	L	H
⑦	-A	-B	-A	-B	-A	-B	-A	-B	H	H
⑧	-B	-A	-B	-A	-B	-A	-B	-A	L	H

FIG. 10



F I G. 1 1

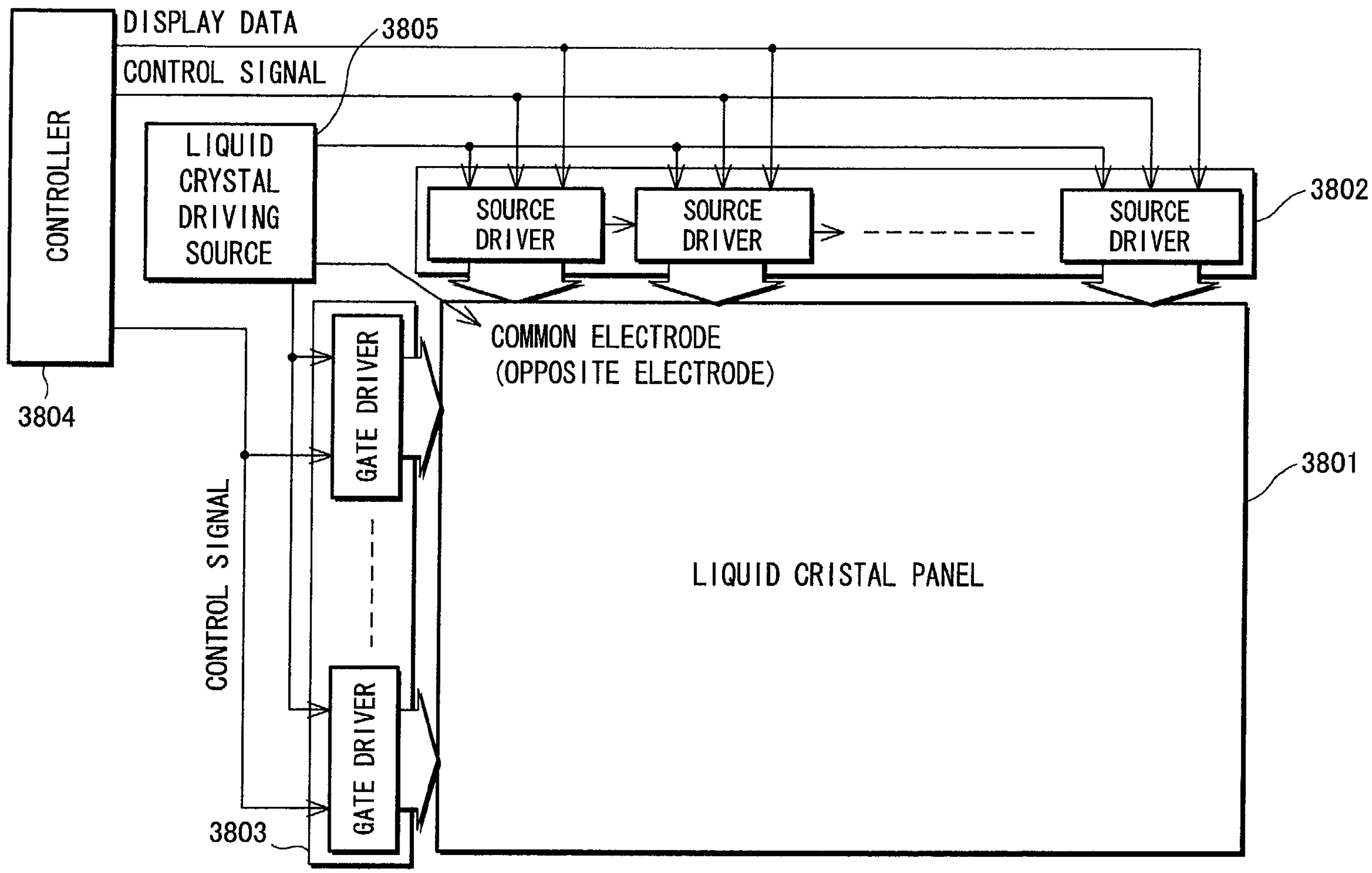

DISPLAY DATA
CONTROL SIGNAL
3805
CONTROLLER
3804
LIQUID CRYSTAL DRIVING SOURCE
SOURCE DRIVER
SOURCE DRIVER
SOURCE DRIVER
3802
COMMON ELECTRODE (OPPOSITE ELECTRODE)
GATE DRIVER
GATE DRIVER
CONTROL SIGNAL
3803
3801
LIQUID CRISTAL PANEL

FIG. 12

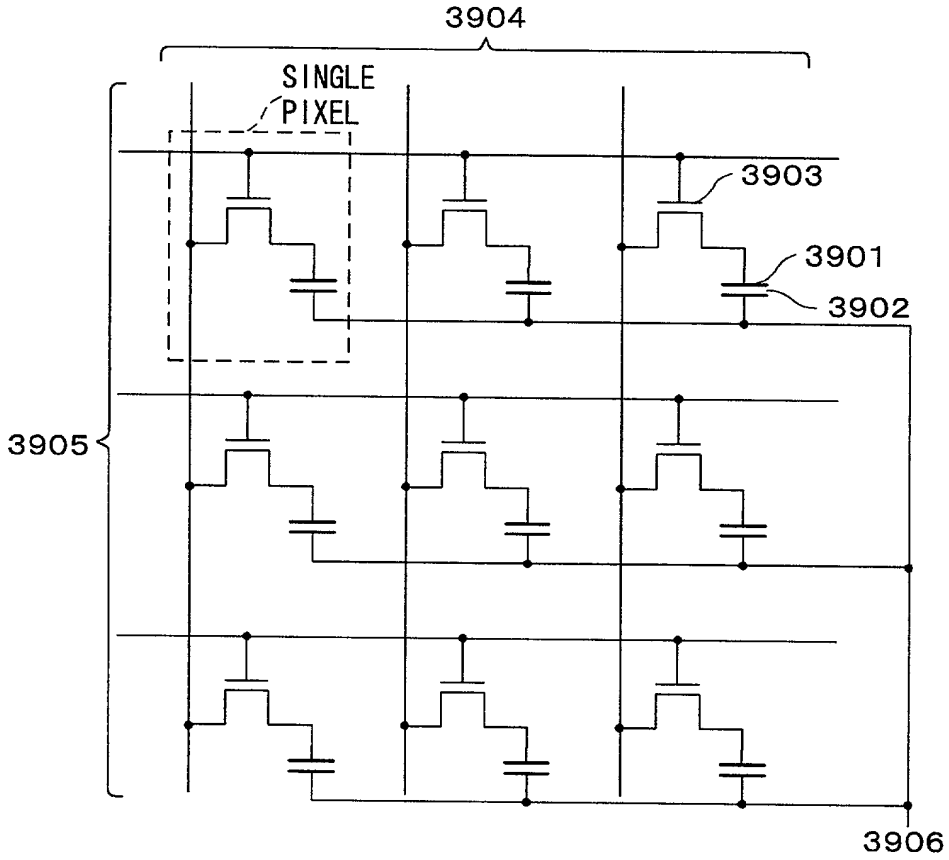


FIG. 13

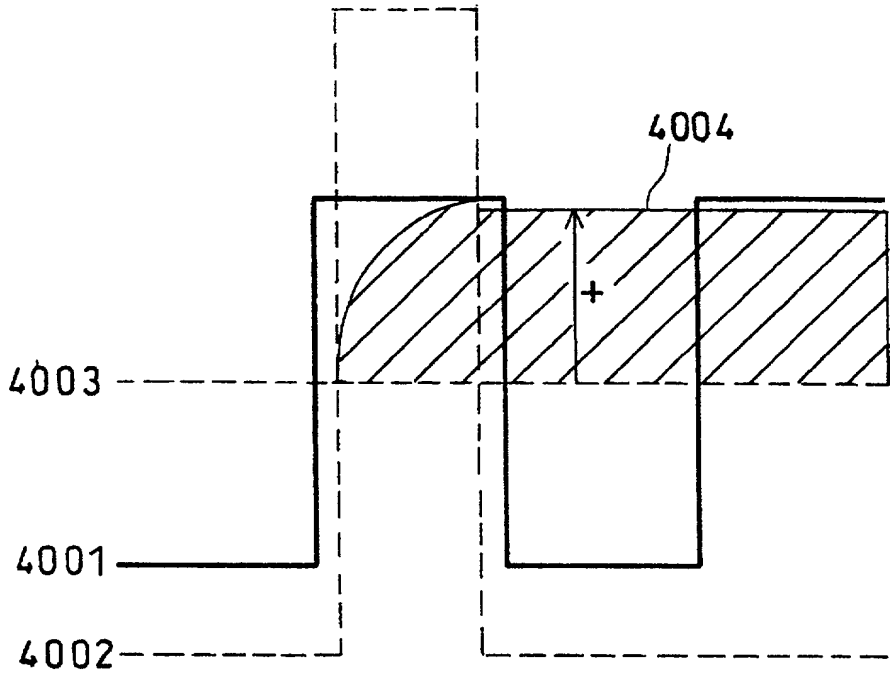


FIG. 14

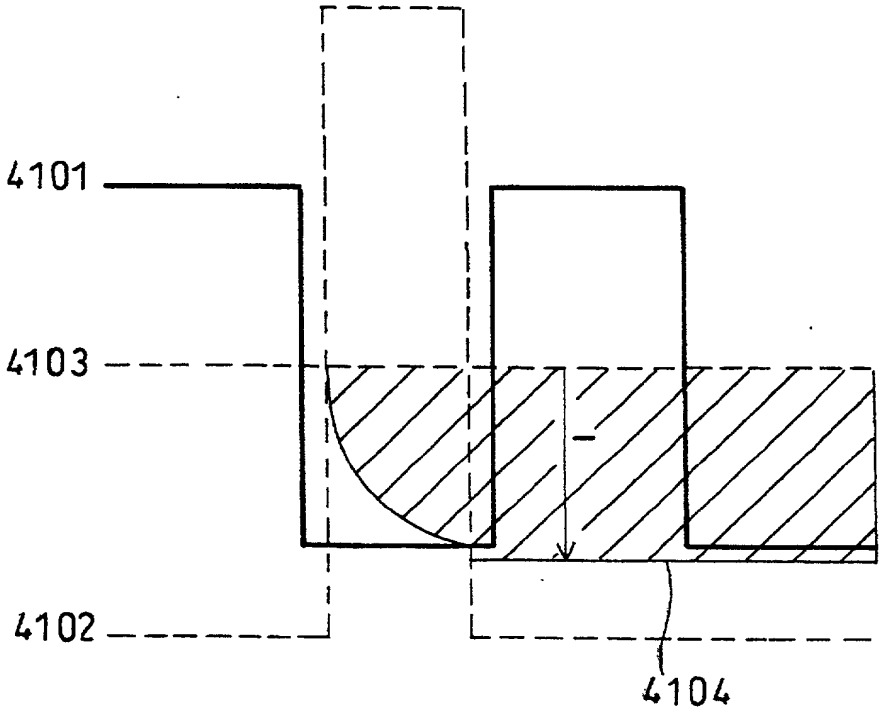


FIG. 15

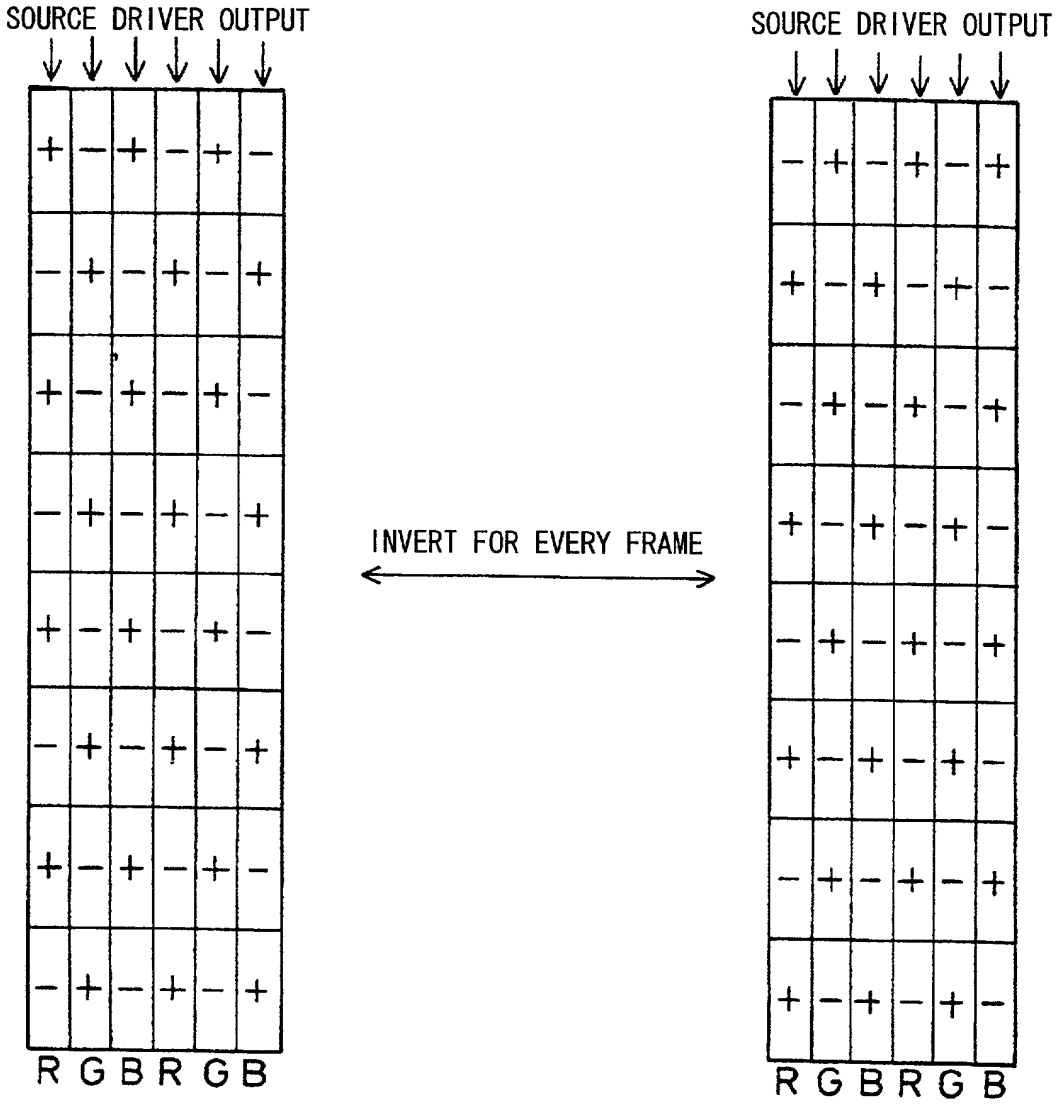

SOURCE DRIVER OUTPUT
R G B R G B
INVERT FOR EVERY FRAME
SOURCE DRIVER OUTPUT
R G B R G B

FIG. 16

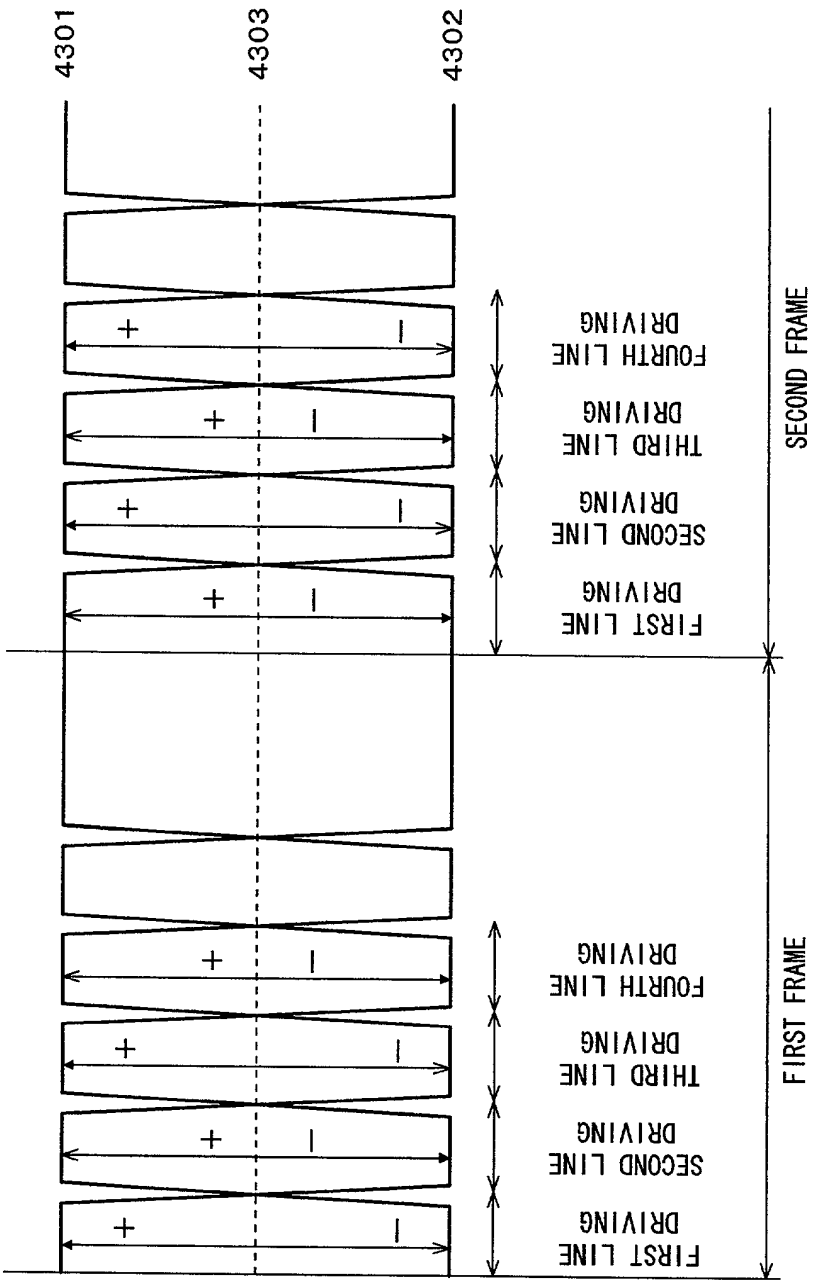

4301
4303
4302
+
−
FOURTH LINE DRIVING
THIRD LINE DRIVING
SECOND LINE DRIVING
FIRST LINE DRIVING
SECOND FRAME
FIRST FRAME

FIG. 17

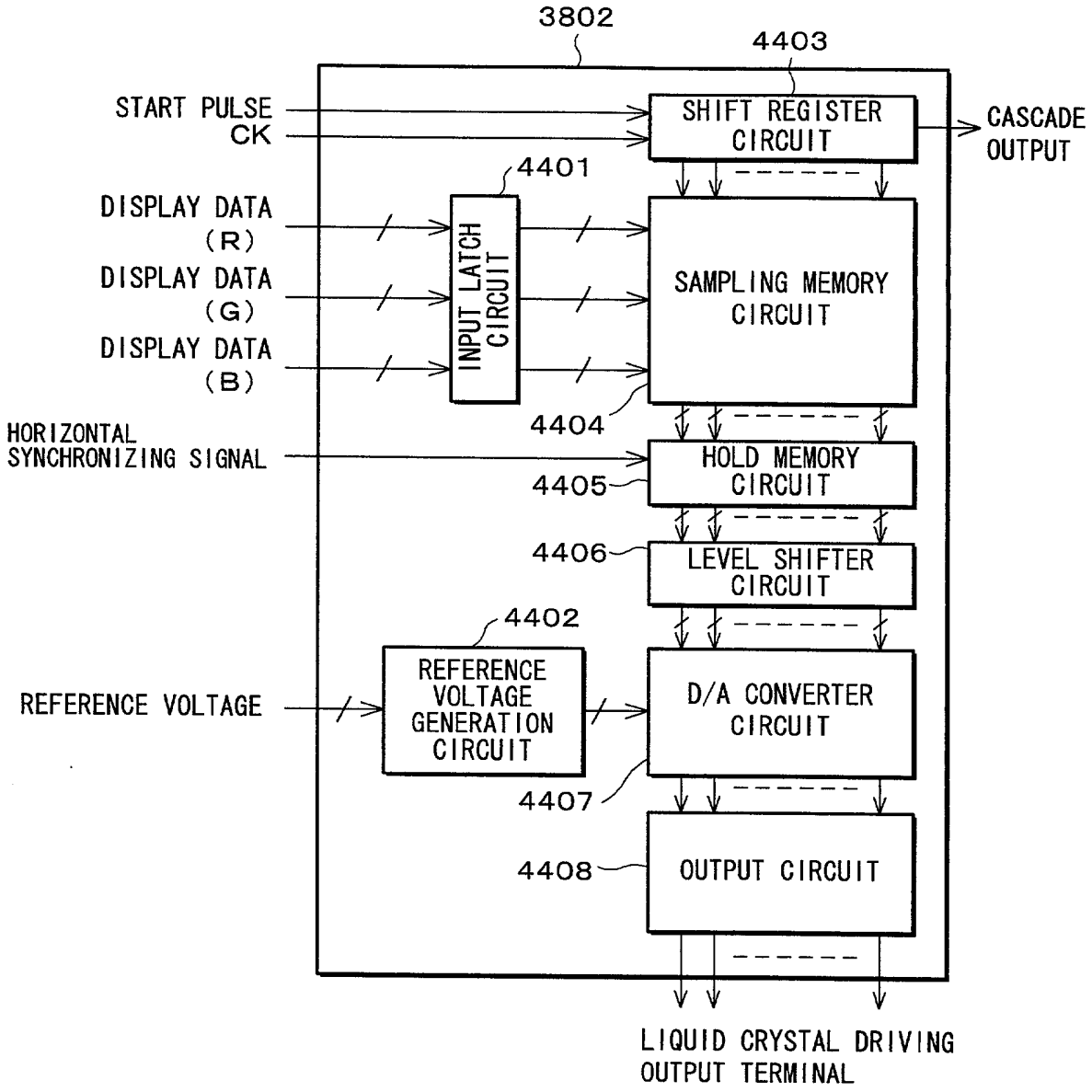

3802
4403
START PULSE
CK
SHIFT REGISTER CIRCUIT
CASCADE OUTPUT
4401
DISPLAY DATA (R)
DISPLAY DATA (G)
DISPLAY DATA (B)
INPUT LATCH CIRCUIT
SAMPLING MEMORY CIRCUIT
4404
HORIZONTAL SYNCHRONIZING SIGNAL
HOLD MEMORY CIRCUIT
4405
4406
LEVEL SHIFTER CIRCUIT
4402
REFERENCE VOLTAGE
REFERENCE VOLTAGE GENERATION CIRCUIT
D/A CONVERTER CIRCUIT
4407
4408
OUTPUT CIRCUIT
LIQUID CRYSTAL DRIVING OUTPUT TERMINAL

FIG. 18 (a)

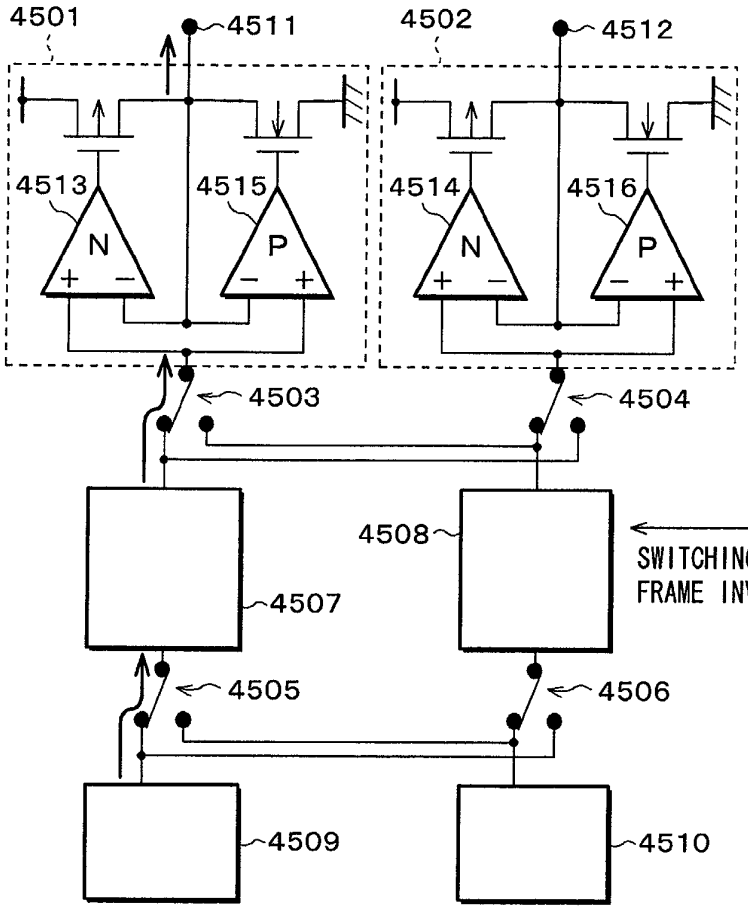
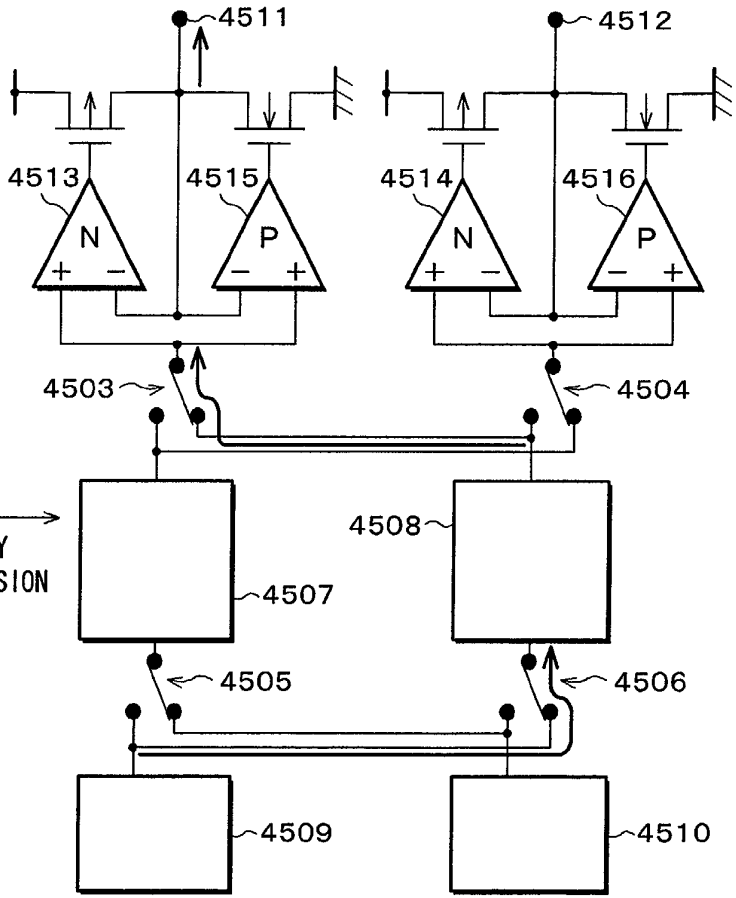


FIG. 18 (b)



SWITCHING BY
FRAME INVERSION

FIG. 19 (a)

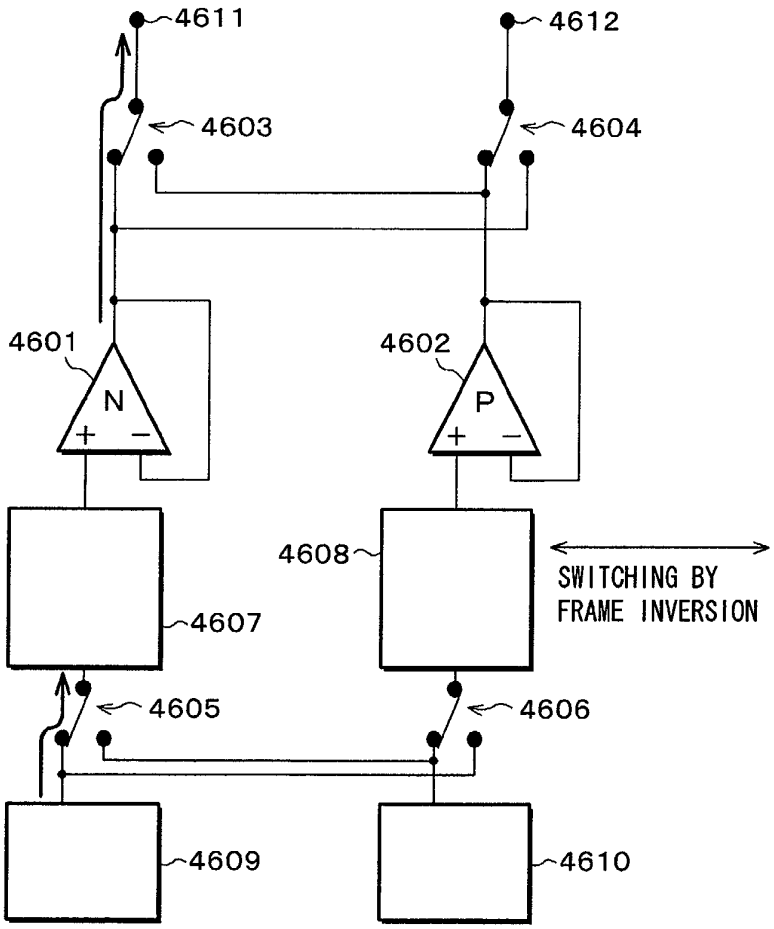
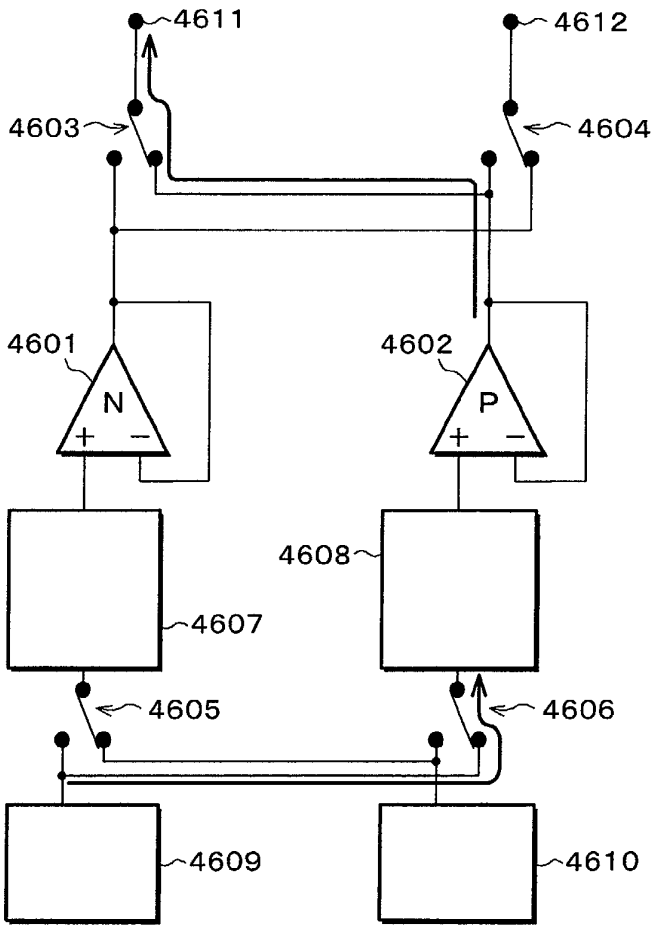
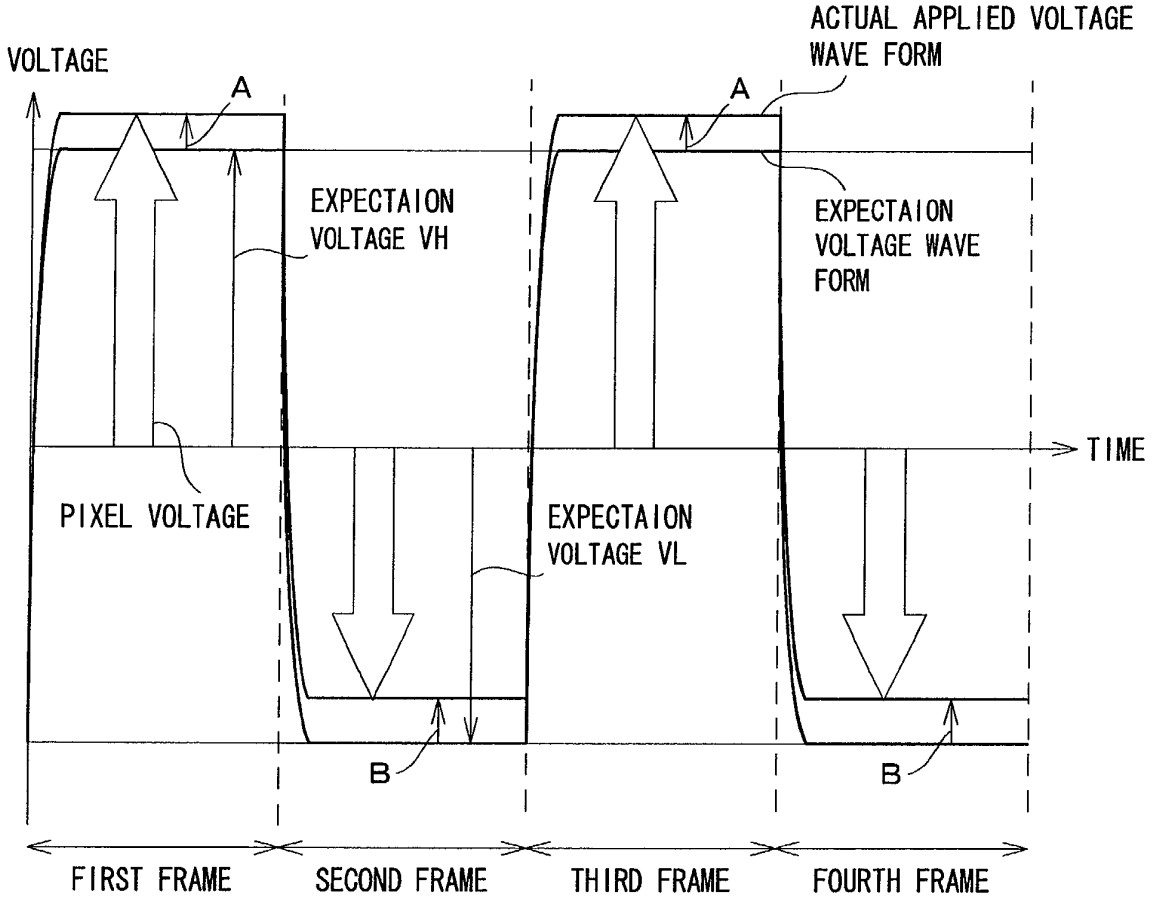


FIG. 19 (b)



SWITCHING BY
FRAME INVERSION

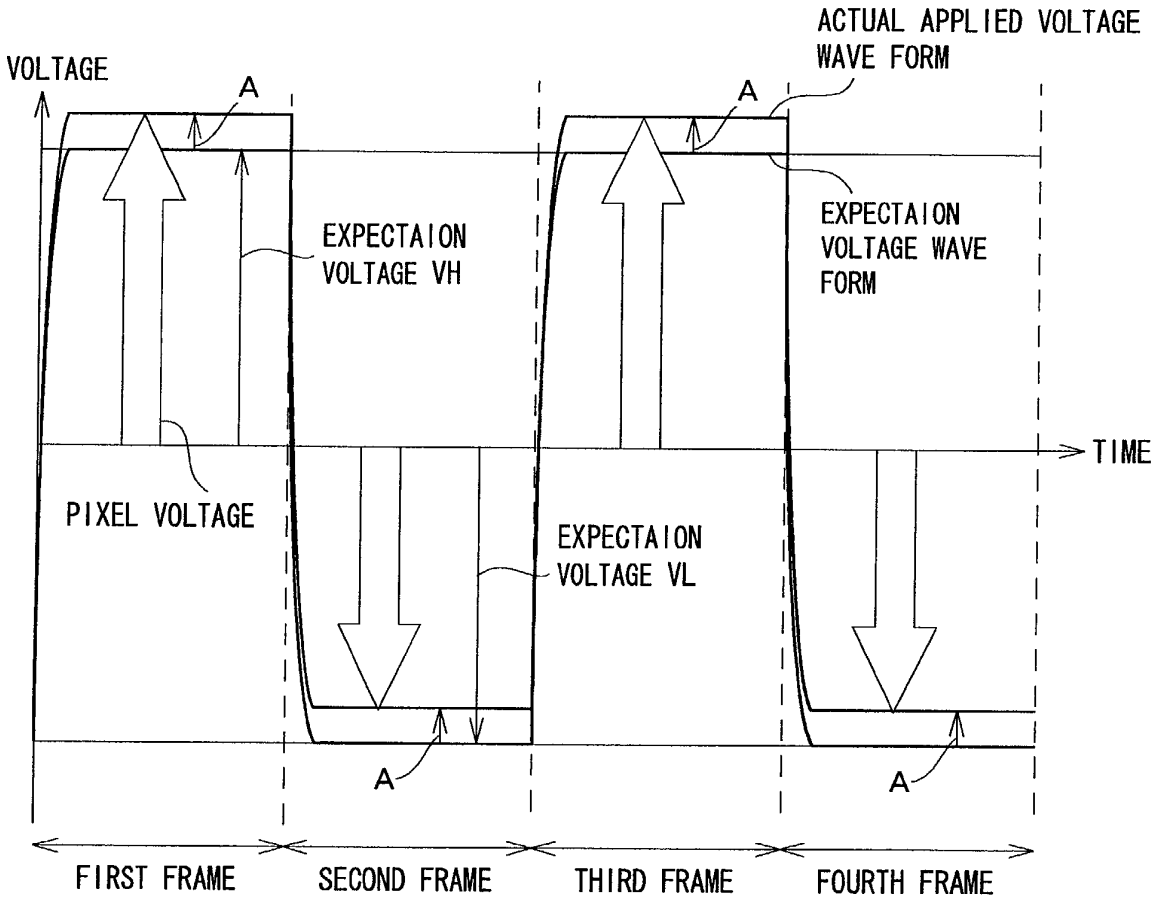
FIG. 20



$$\text{AVERAGE PIXEL VOLTAGES} = \{(VH+A)+(VL-B)+(VH+A)+(VL-B)\} \div 4$$

$$= \frac{VH+VL}{2} + \frac{A-B}{2}$$

FIG. 21



$$\text{AVERAGE PIXEL VOLTAGES} = \{(VH+A)+(VL-A)+(VH+A)+(VL-A)\} \div 4$$

$$= \frac{VH+VL}{2}$$

FIG. 22

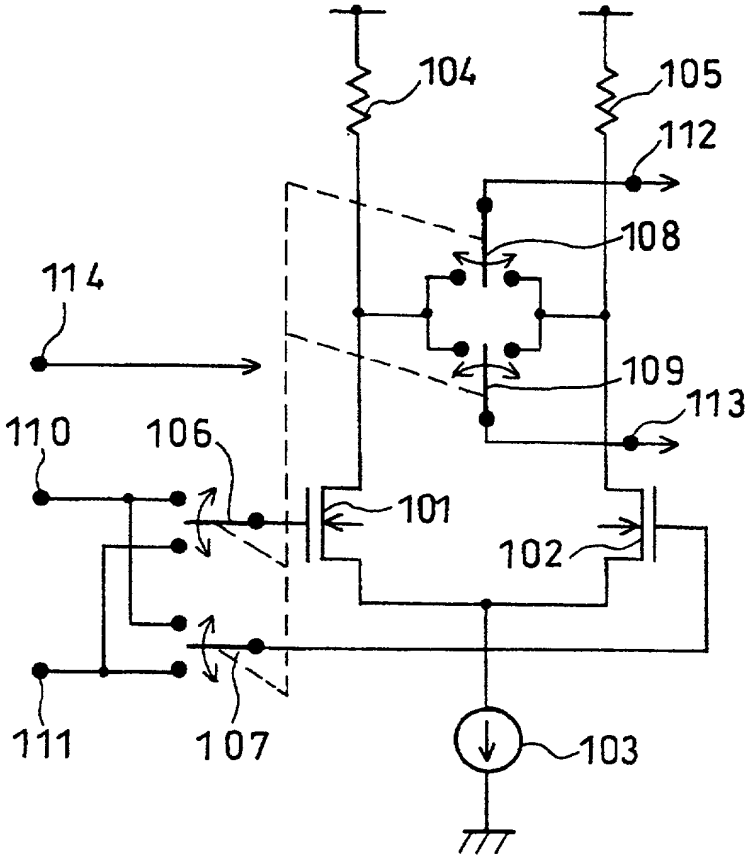


FIG. 23

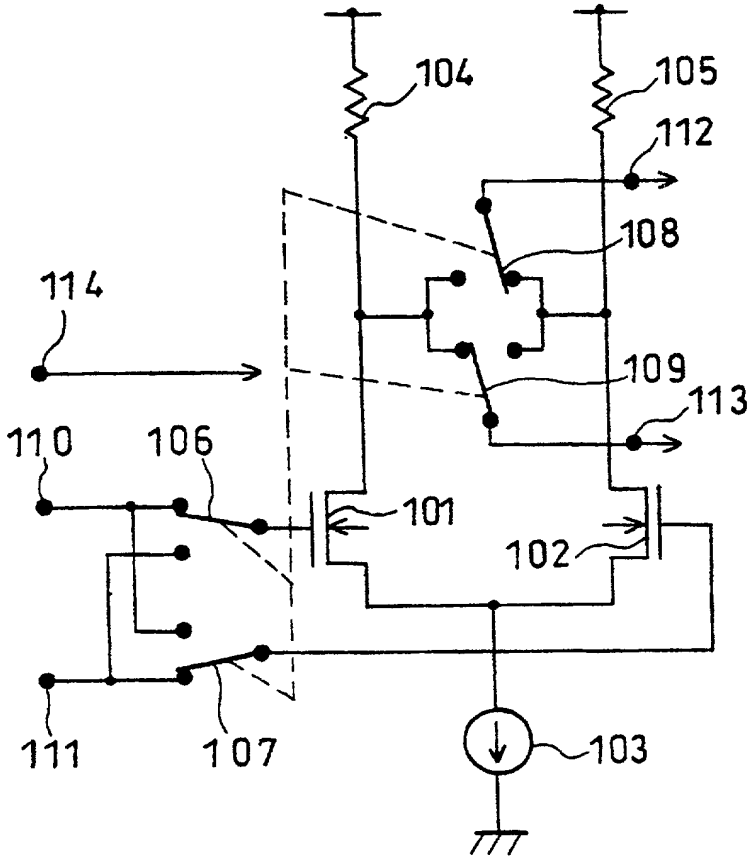


FIG. 24

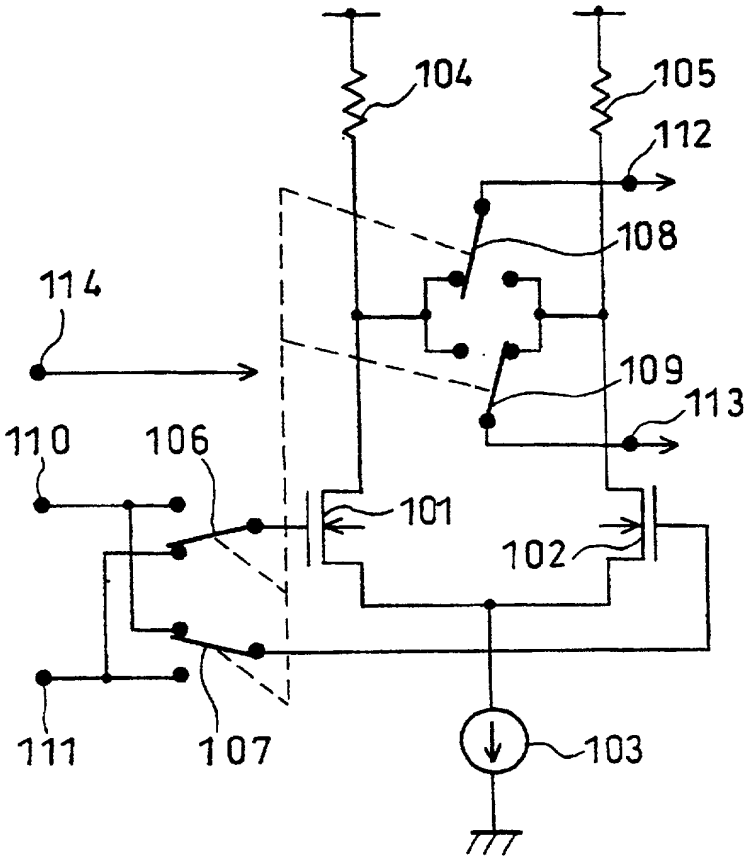


FIG. 25

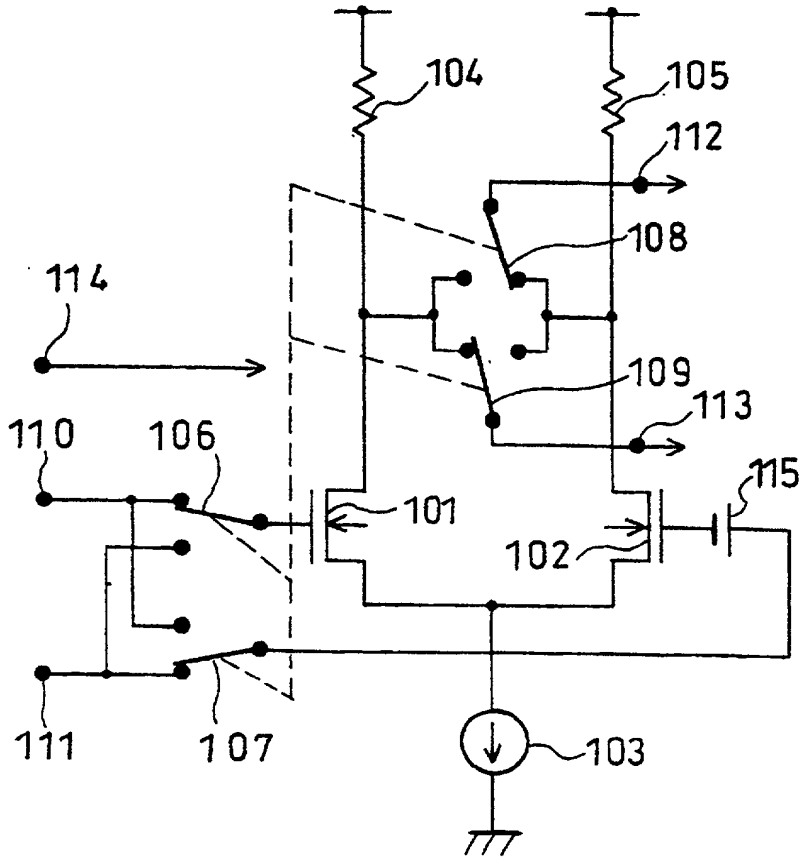


FIG. 26

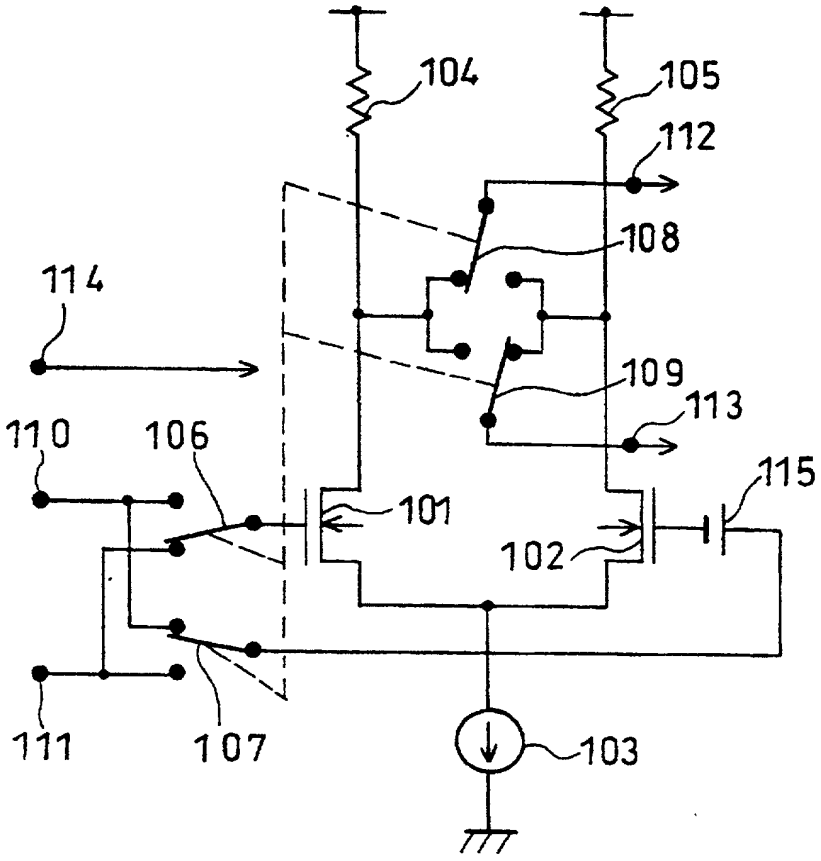


FIG. 27

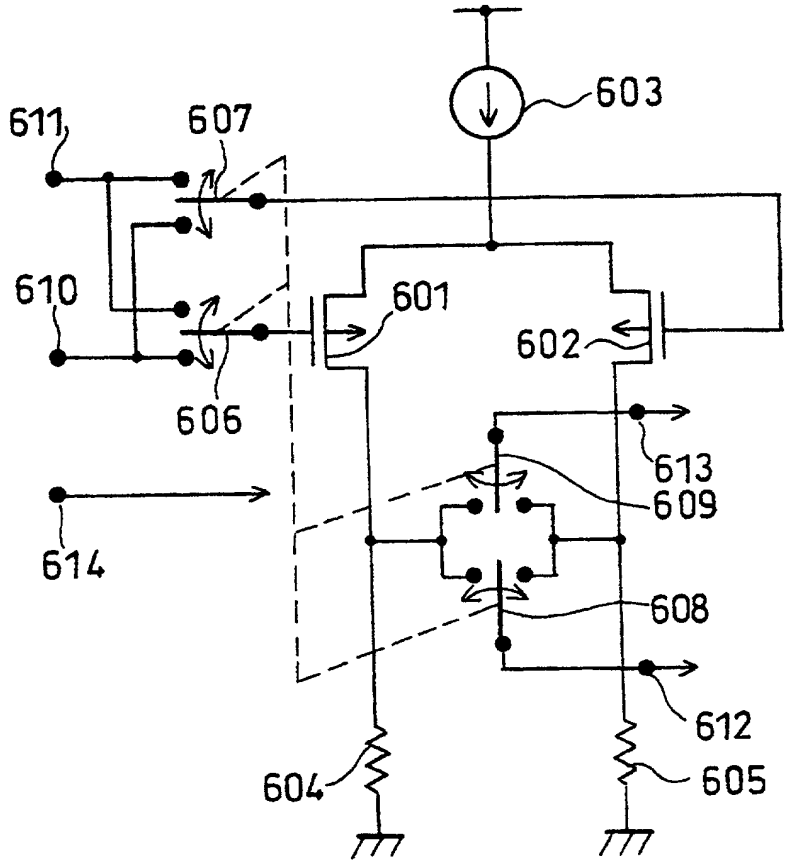


FIG. 28

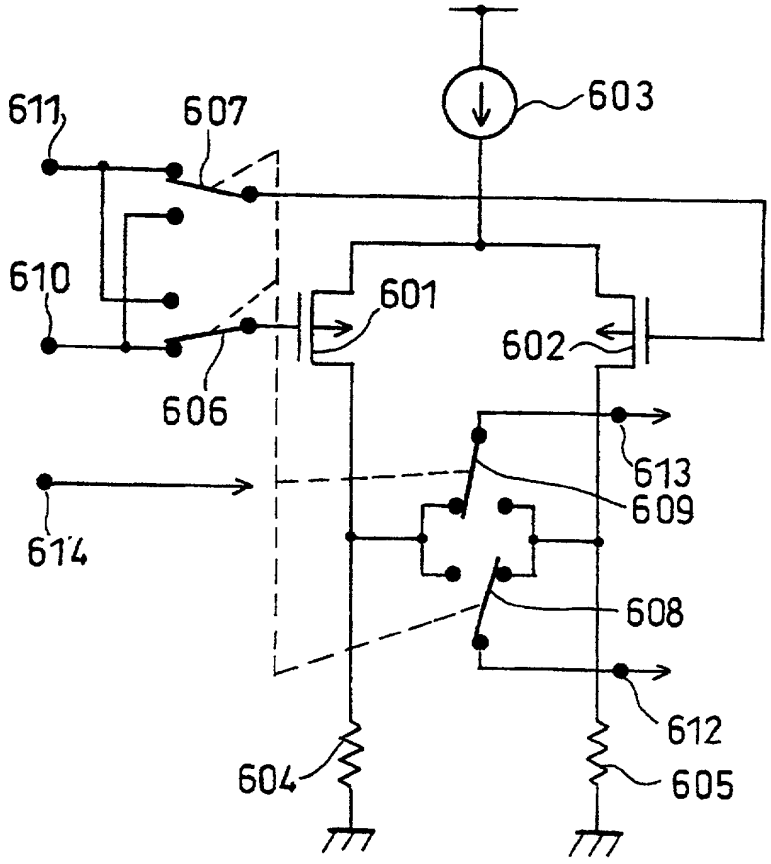


FIG. 29

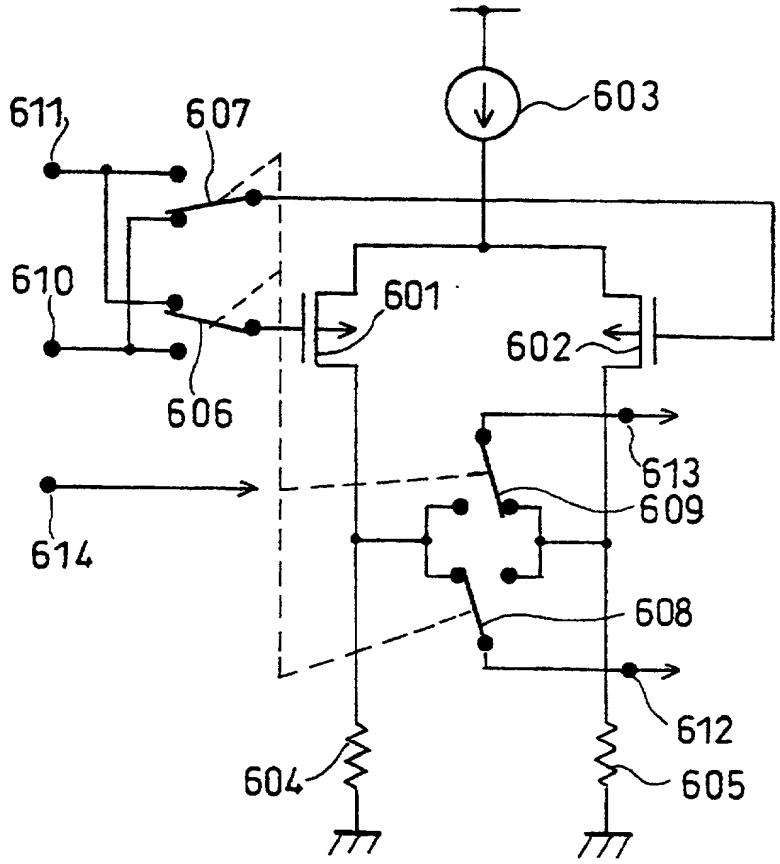


FIG. 30

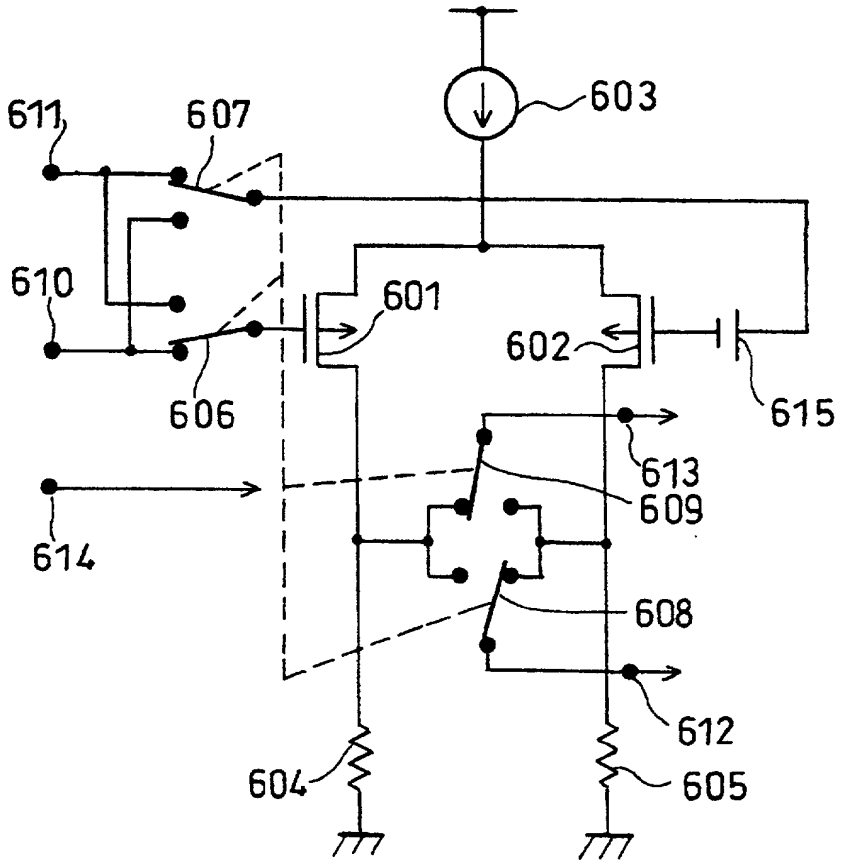


FIG. 31

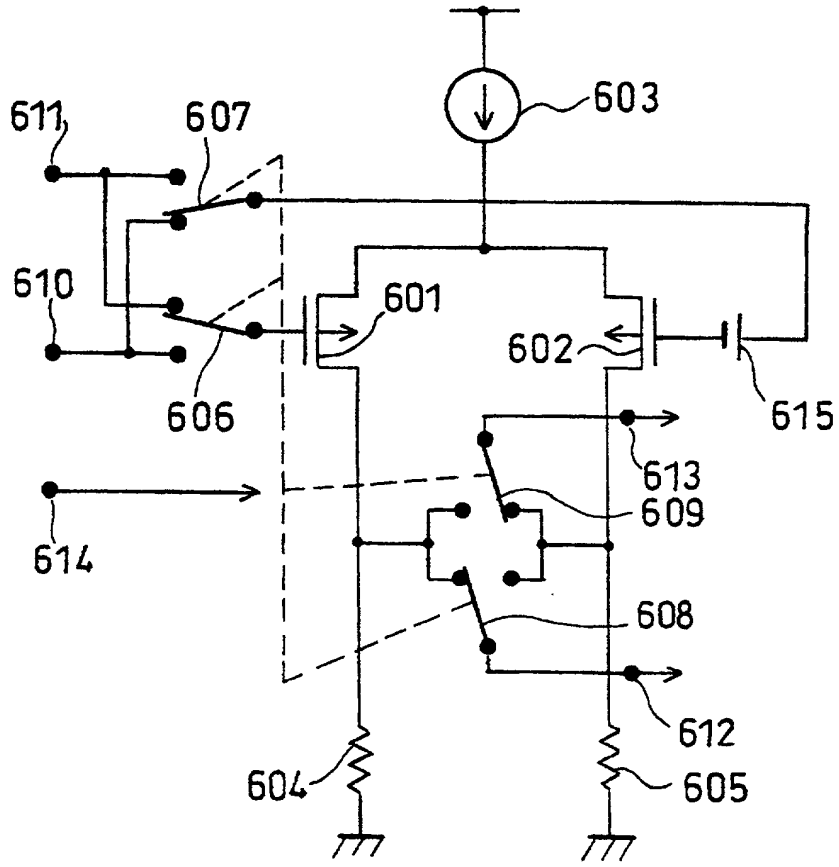


FIG. 32

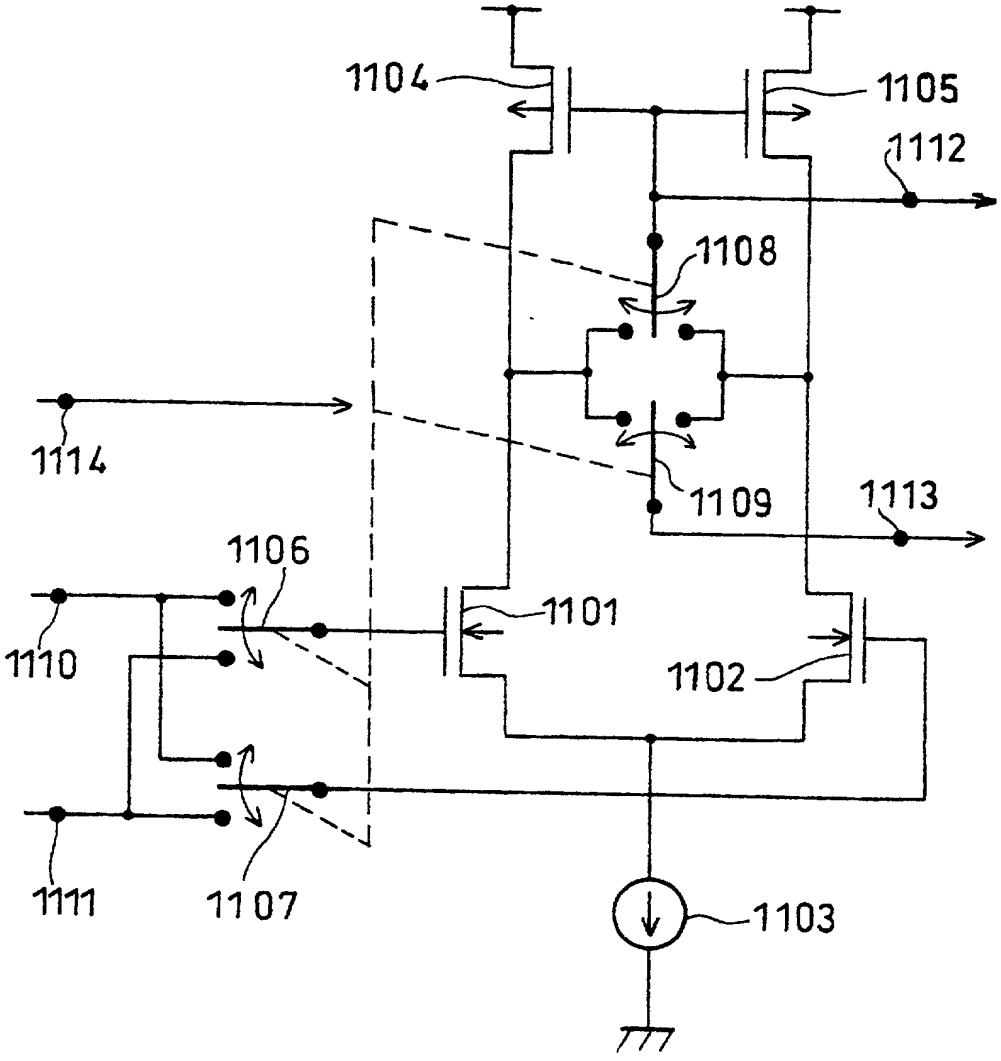

1104
1105
1112
1108
1114
1109
1113
1106
1101
1110
1102
1111
1107
1103

FIG. 33

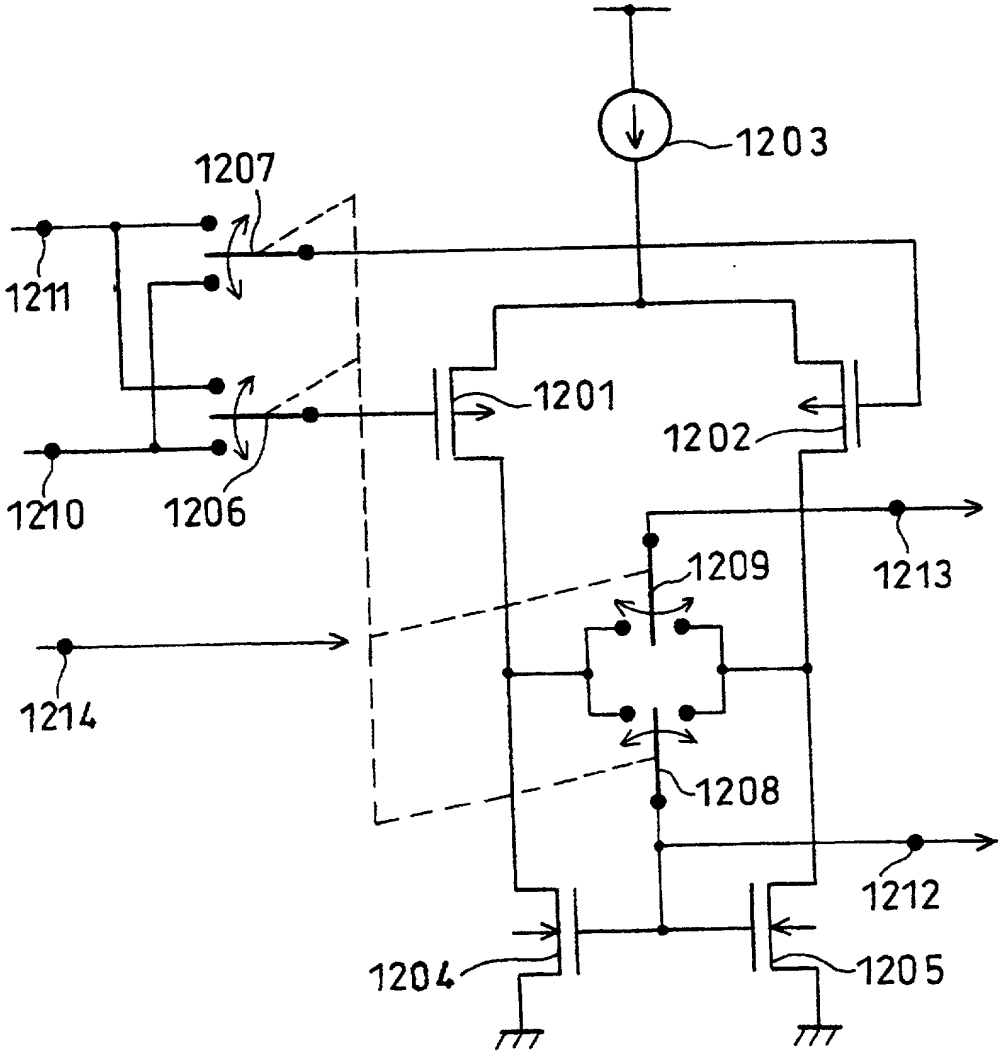

1203
1207
1211
1201
1202
1210
1206
1209
1213
1214
1208
1212
1204
1205

FIG. 34

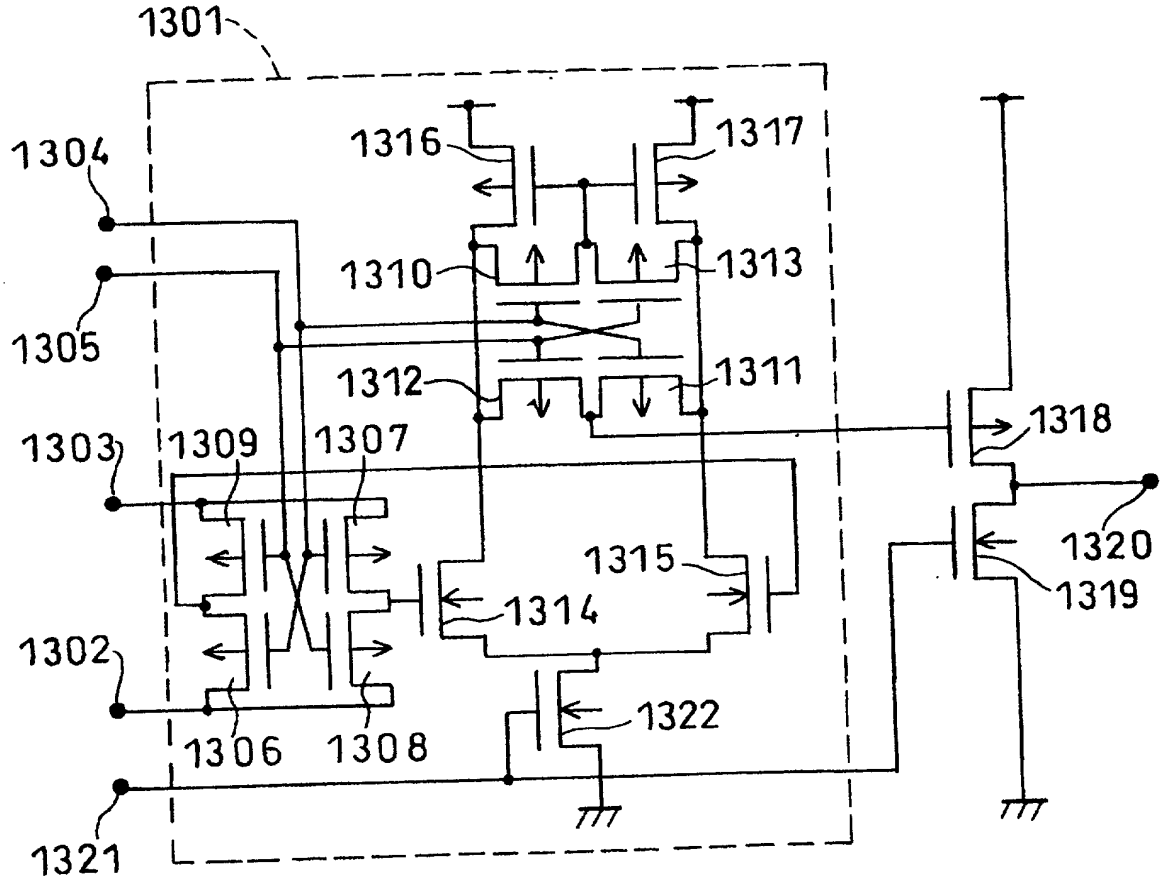

1301
1304
1316
1317
1310
1313
1305
1312
1311
1318
1303
1309
1307
1315
1320
1314
1319
1302
1322
1306
1308
1321

FIG. 35

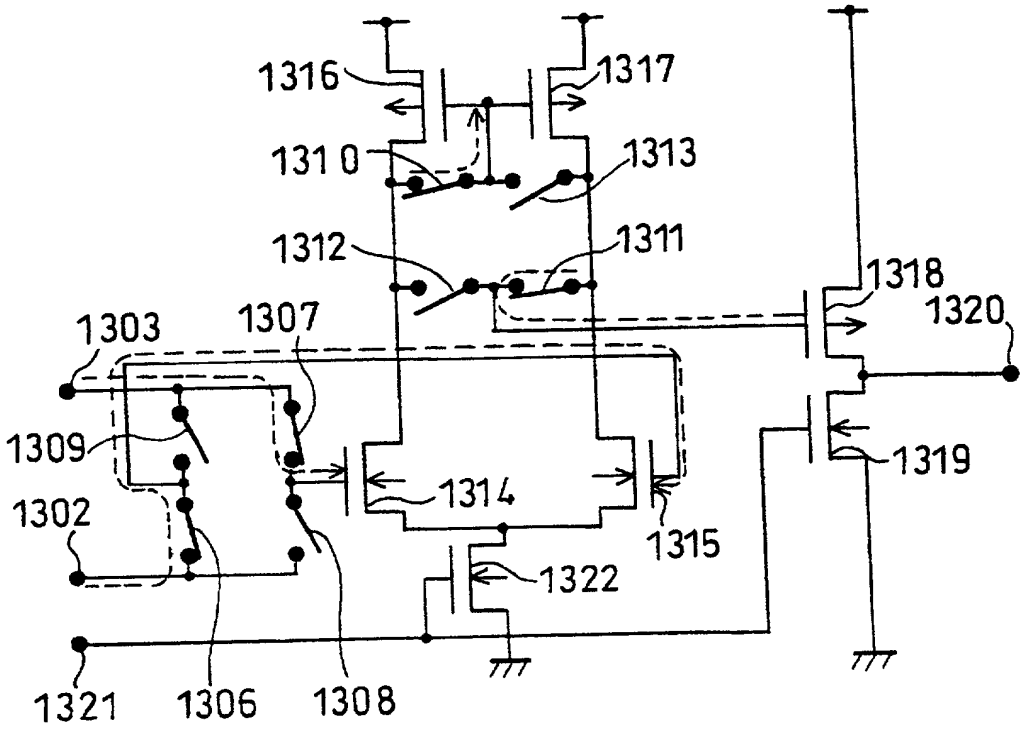

1316
1317
1310
1313
1312
1311
1318
1320
1303
1307
1309
1319
1314
1302
1315
1322
1321
1306
1308

FIG. 36

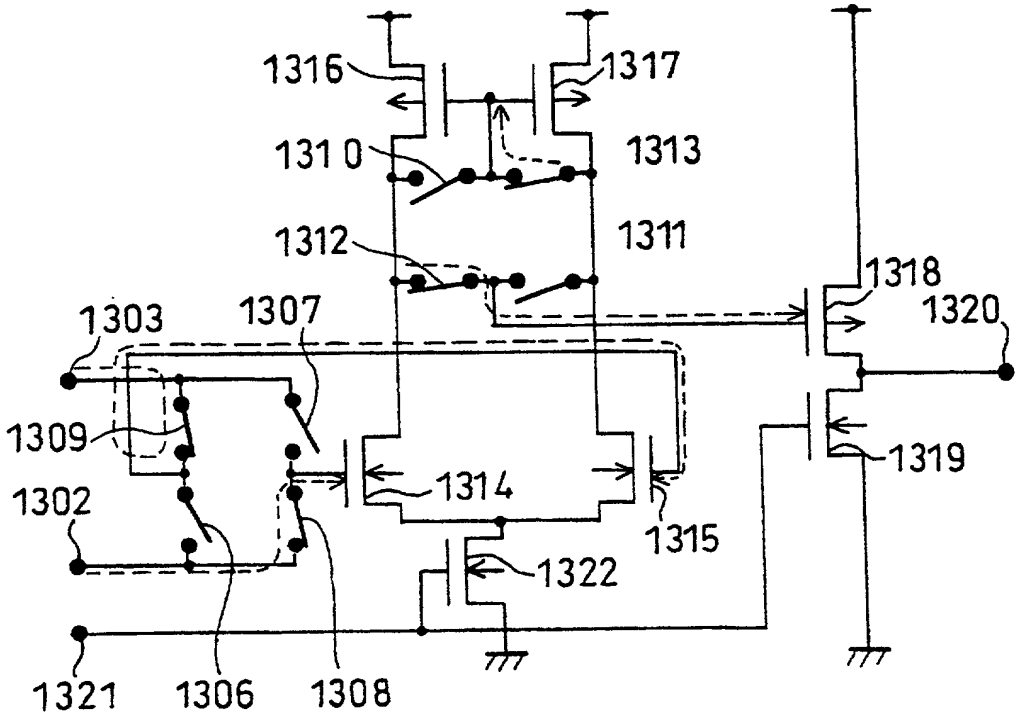

1316
1317
1310
1313
1312
1311
1318
1320
1303
1307
1309
1319
1314
1302
1315
1322
1321
1306
1308

FIG. 37

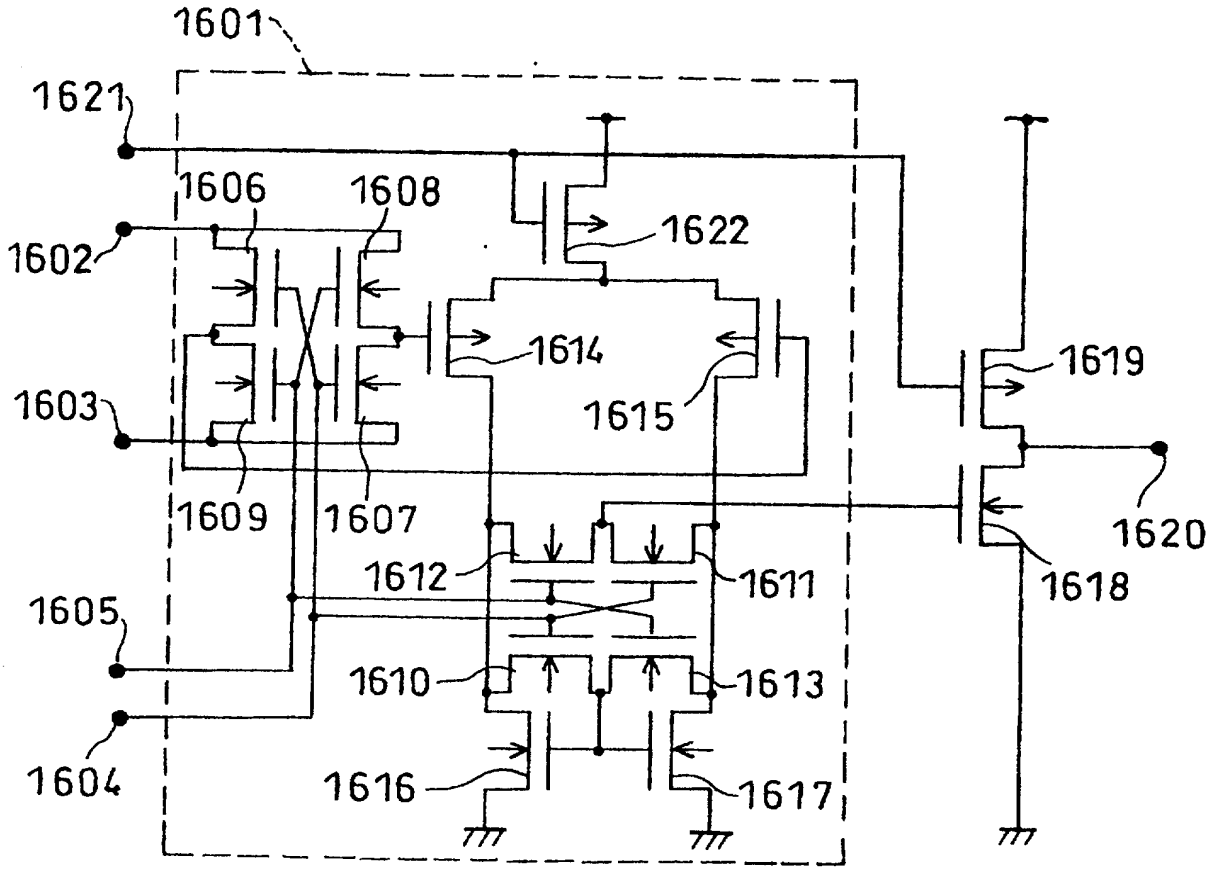
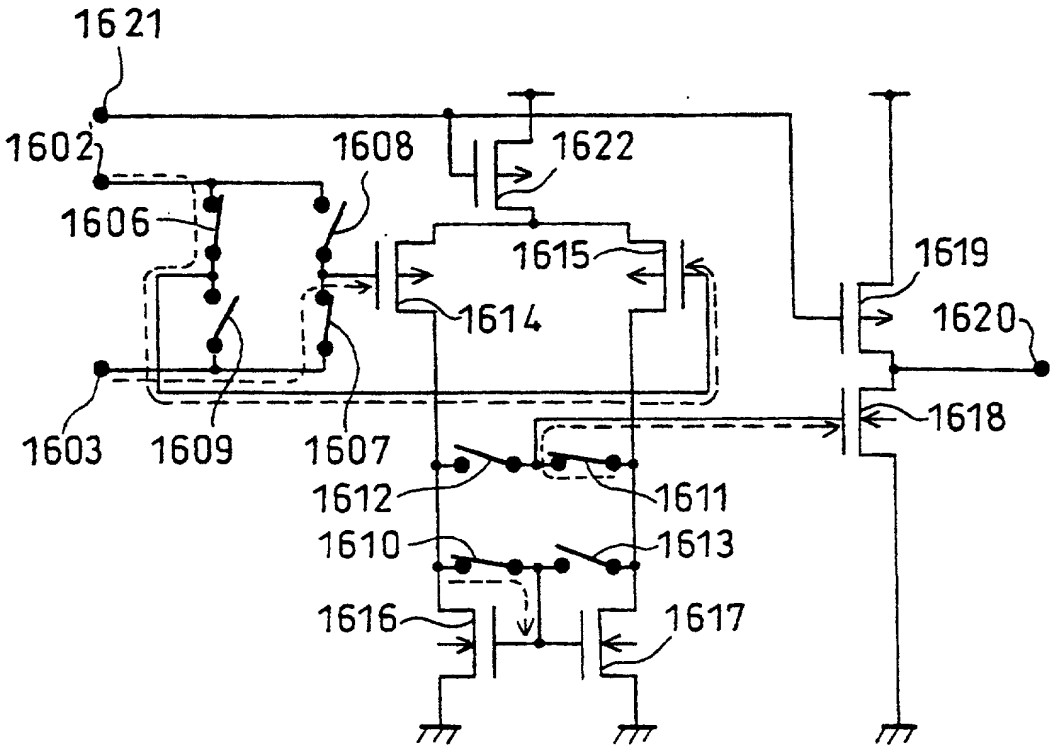

1601
1621
1606
1608
1602
1622
1614
1619
1603
1615
1609
1607
1620
1612
1611
1618
1605
1610
1613
1604
1616
1617

FIG. 38


1621
1602
1608
1622
1606
1615
1619
1614
1620
1603
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1607
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1612
1611
1610
1613
1616
1617

FIG. 39

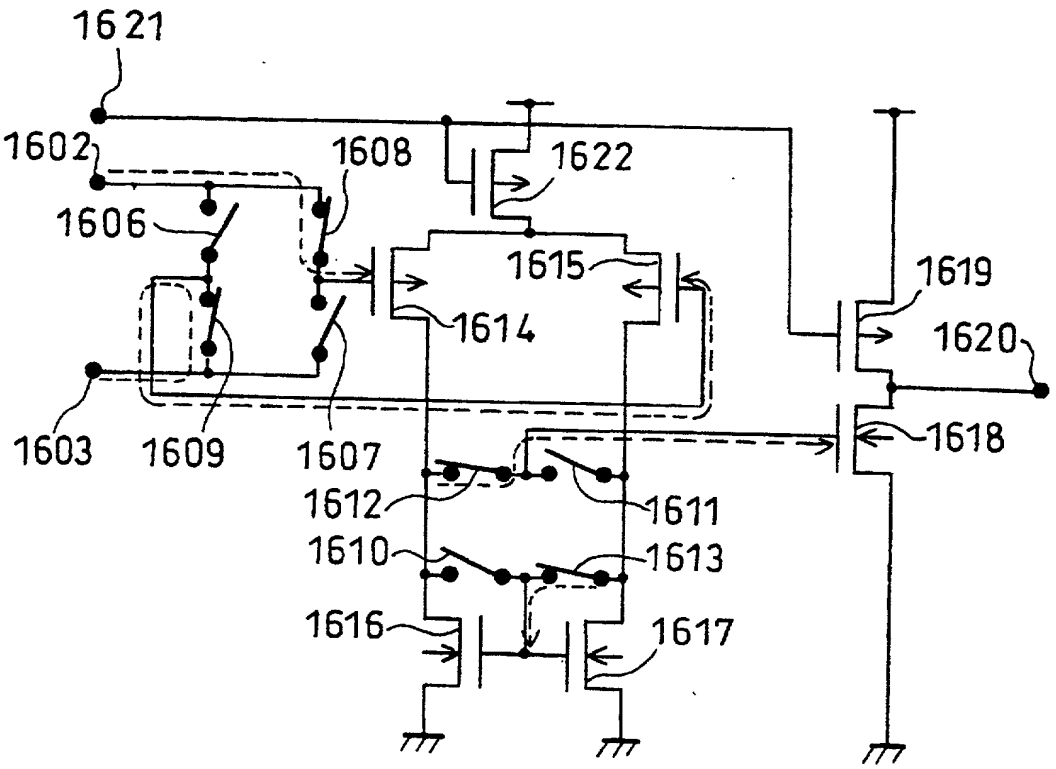

1621
1602
1608
1622
1606
1615
1619
1614
1620
1603
1609
1607
1618
1612
1611
1610
1613
1616
1617

FIG. 40

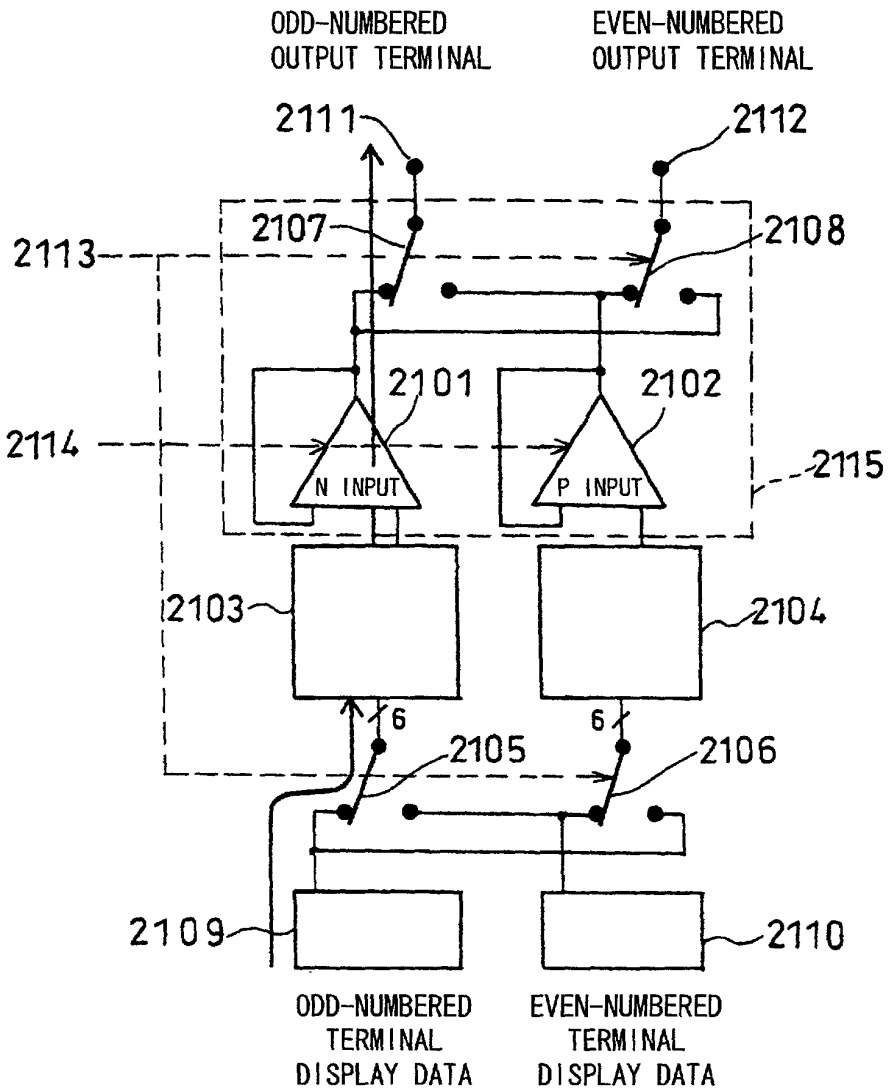

ODD-NUMBERED
OUTPUT TERMINAL
EVEN-NUMBERED
OUTPUT TERMINAL
2111
2112
2107
2108
2113
2101
2102
2114
N INPUT
P INPUT
2115
2103
2104
6
6
2105
2106
2109
2110
ODD-NUMBERED
TERMINAL
DISPLAY DATA
EVEN-NUMBERED
TERMINAL
DISPLAY DATA

FIG. 41

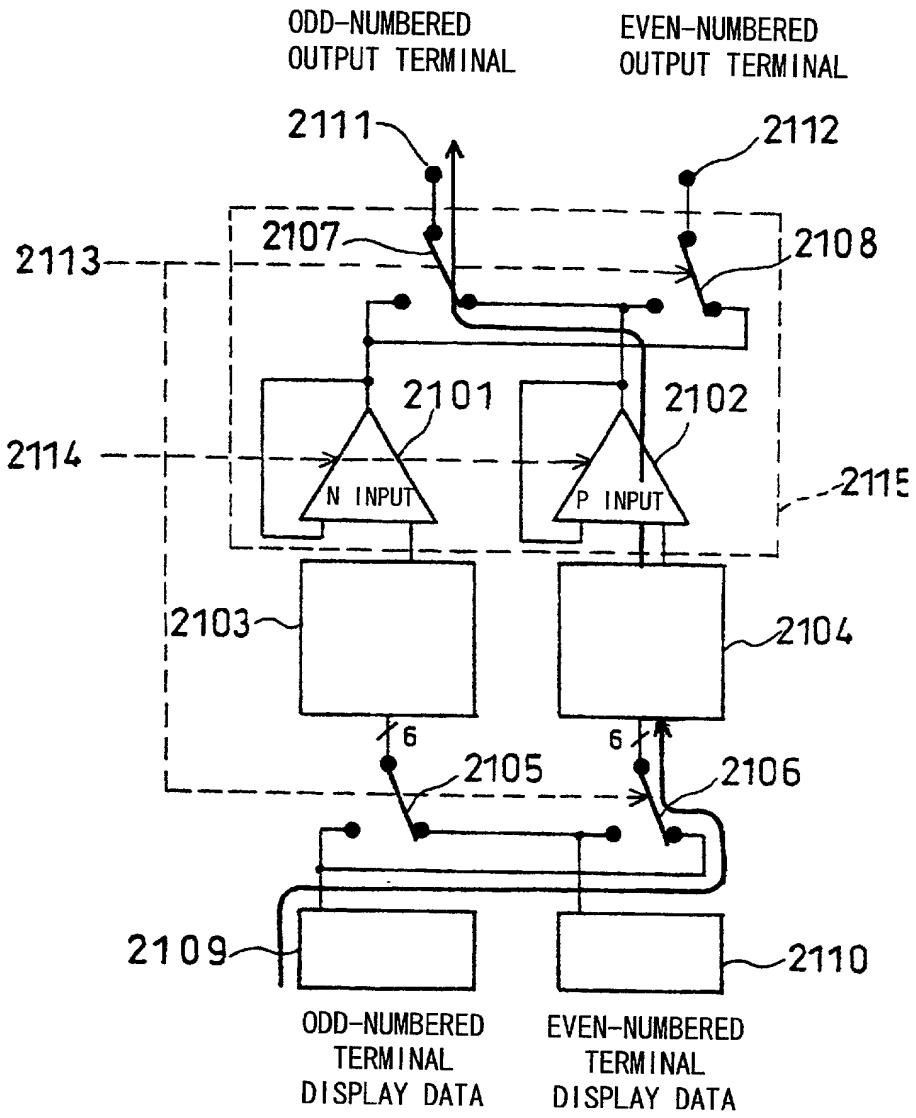
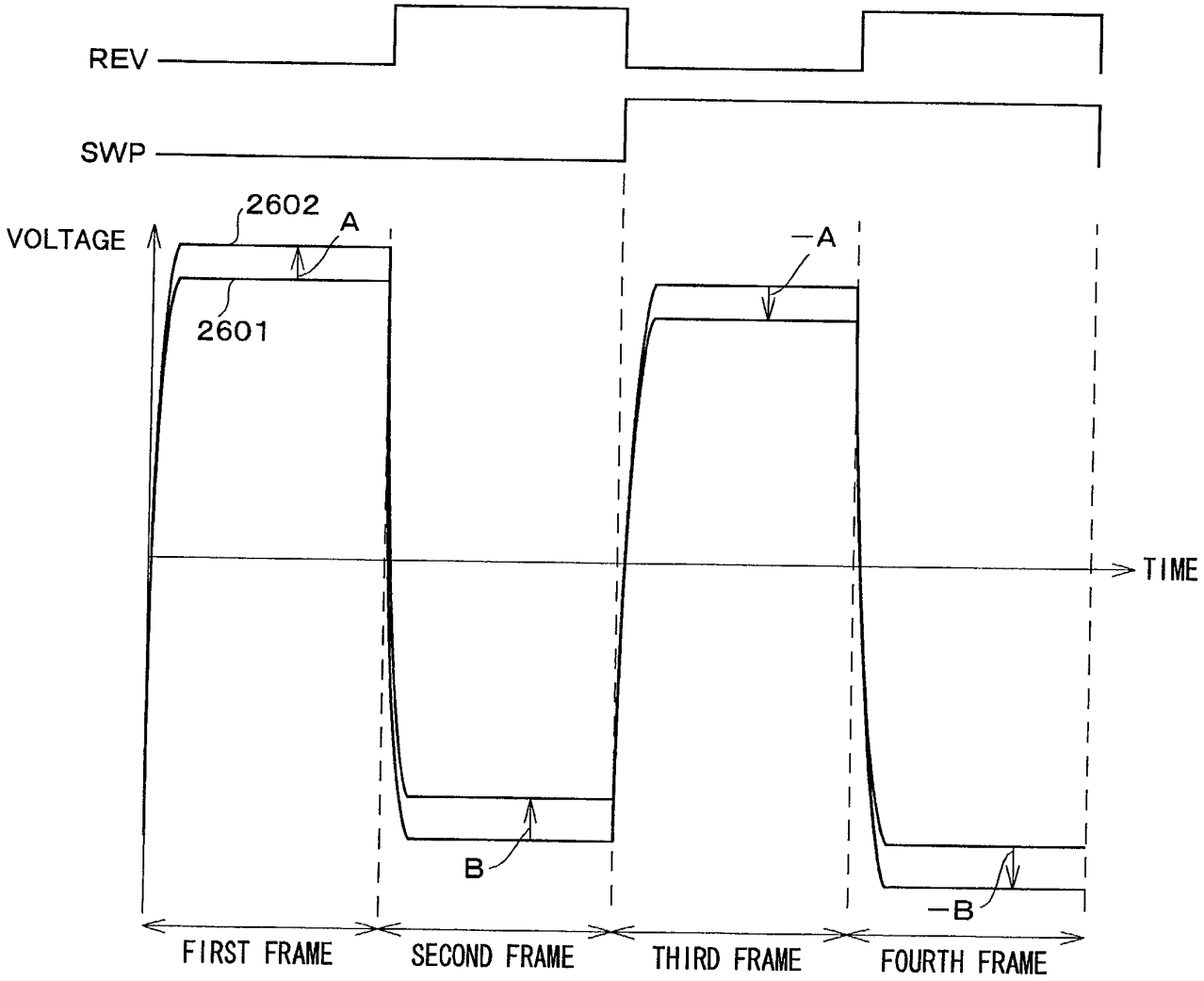

ODD-NUMBERED
OUTPUT TERMINAL
EVEN-NUMBERED
OUTPUT TERMINAL
2111
2112
2107
2108
2113
2101
2102
2114
N INPUT
P INPUT
2115
2103
2104
6
6
2105
2106
2109
2110
ODD-NUMBERED
TERMINAL
DISPLAY DATA
EVEN-NUMBERED
TERMINAL
DISPLAY DATA

FIG. 42


REV
SWP
VOLTAGE
2602
2601
A
-A
B
-B
TIME
FIRST FRAME
SECOND FRAME
THIRD FRAME
FOURTH FRAME